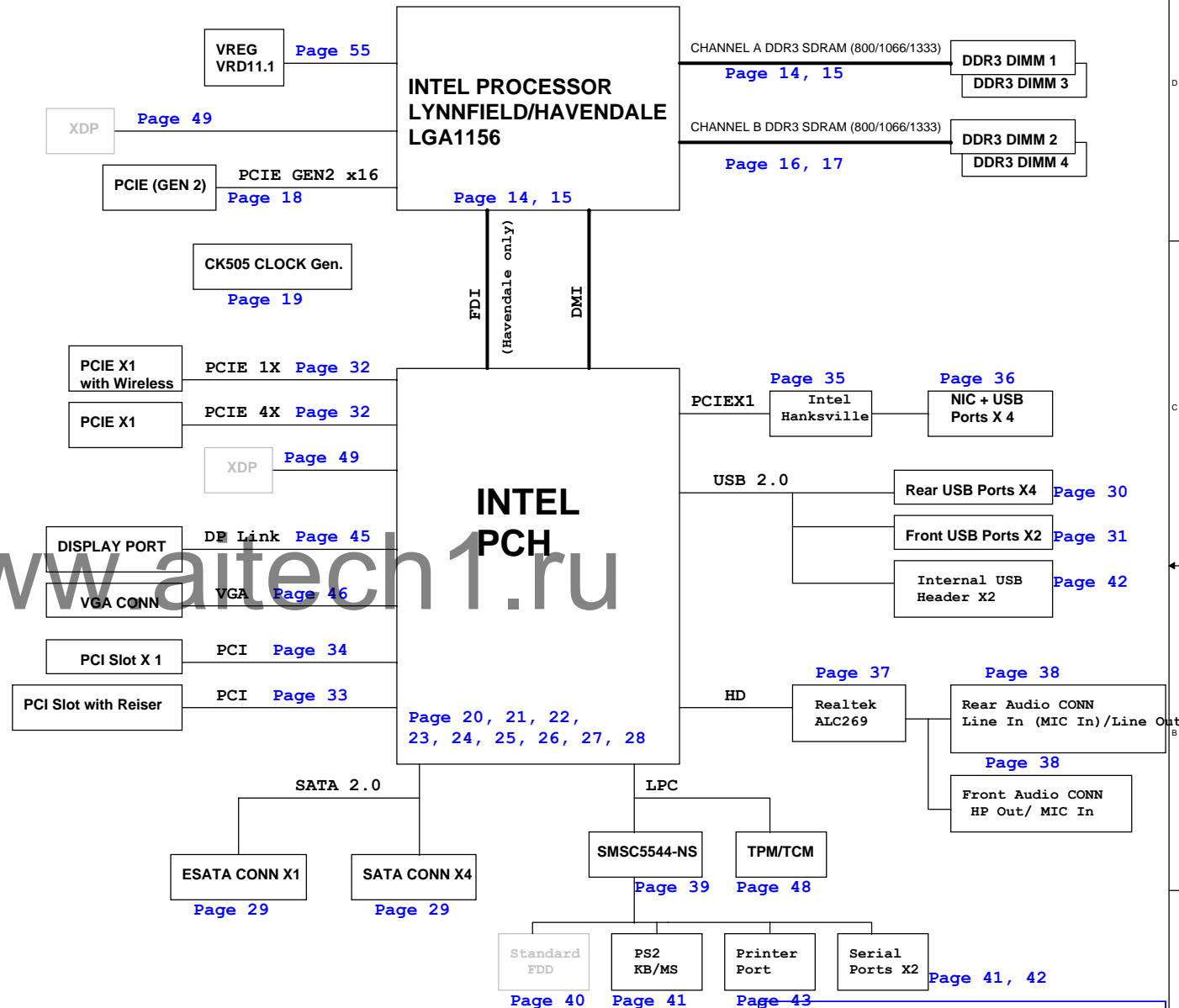


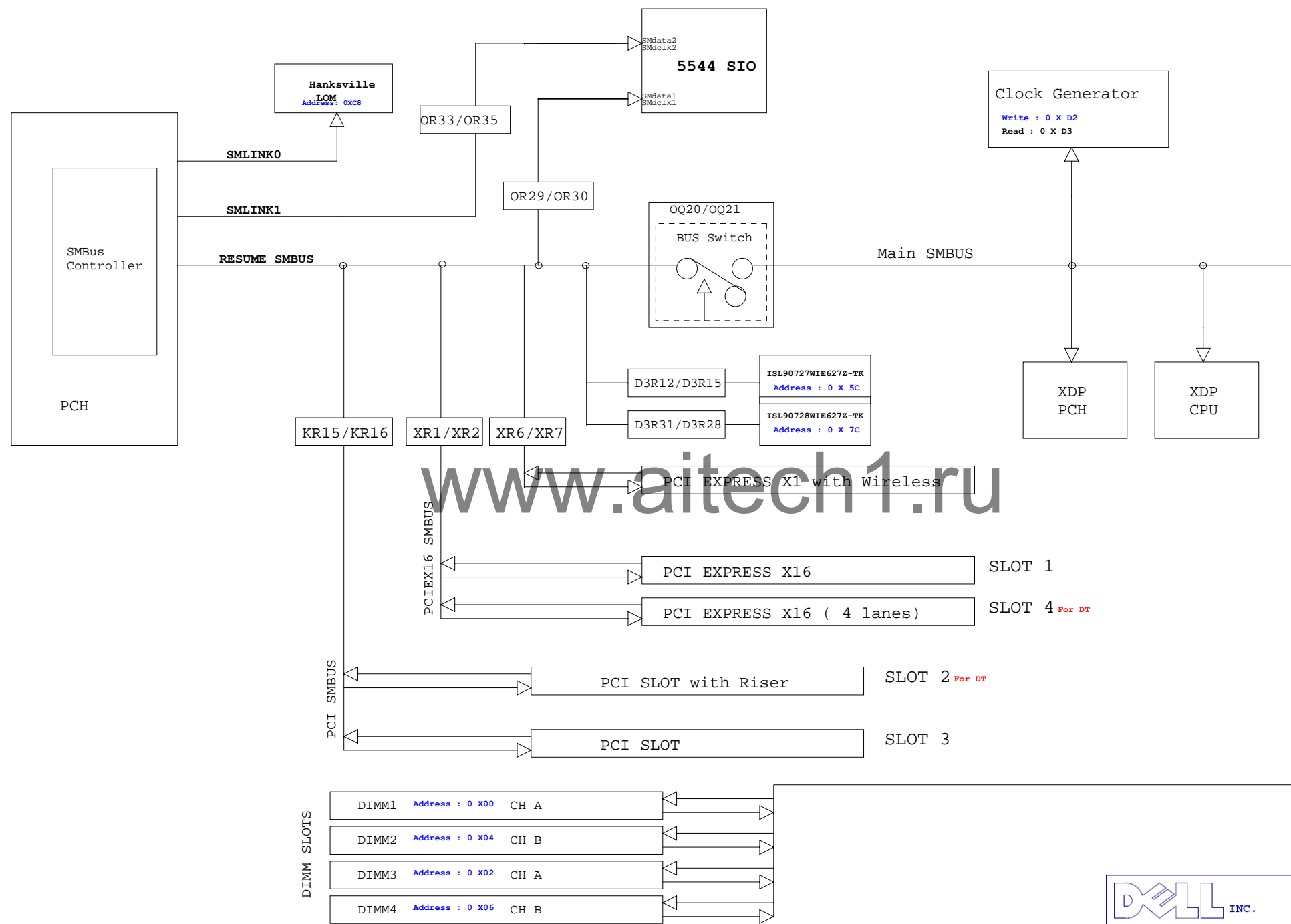
1. Index / Block diagram
2. SMBus MAP
3. Clock Distribution
4. Power Delivery Map
5. Power On Sequence
6. Reset / Power Good Map
7. GPIO/IRQ/IDSEL TABLE
- 8-13. CPU
- 14-15. DDR3:CHA
- 16-17 DDR3:CHB
- 18 .PCIE X16 SLOT
19. CLOCK GEN
- 20-28. PCH
29. SATA CONNECTOR
30. REAR USB CONNECTOR
31. FRONT USB HEADER
32. PCIE X1 SLOT
- 33-34. PCI SLOT
35. LAN:INTEL HANKSVILLE
36. LAN:CONNECTOR WITH USB/POWER
- 37-38. AUDIO:ALC269
- 39-40. SIO:SMSC5544NS
41. COM Port/PS2
42. Front I/O & COM2 HDR
43. PRT Port
44. FAN
45. DISPLAY PORT
46. VGA
47. SPI
48. TPM/TCM
49. XDP
50. BUZ / CLR PSWD/LPC DEBUG
51. ATX Power CONN /Floppy
52. POWER SEQUENCE
- 53-54. POWER:LINEAR POWER REGULATOR
- 55-58. POWER:SWITCH POWER REGULATOR
59. EMI
60. Change List
61. GPIO PIN



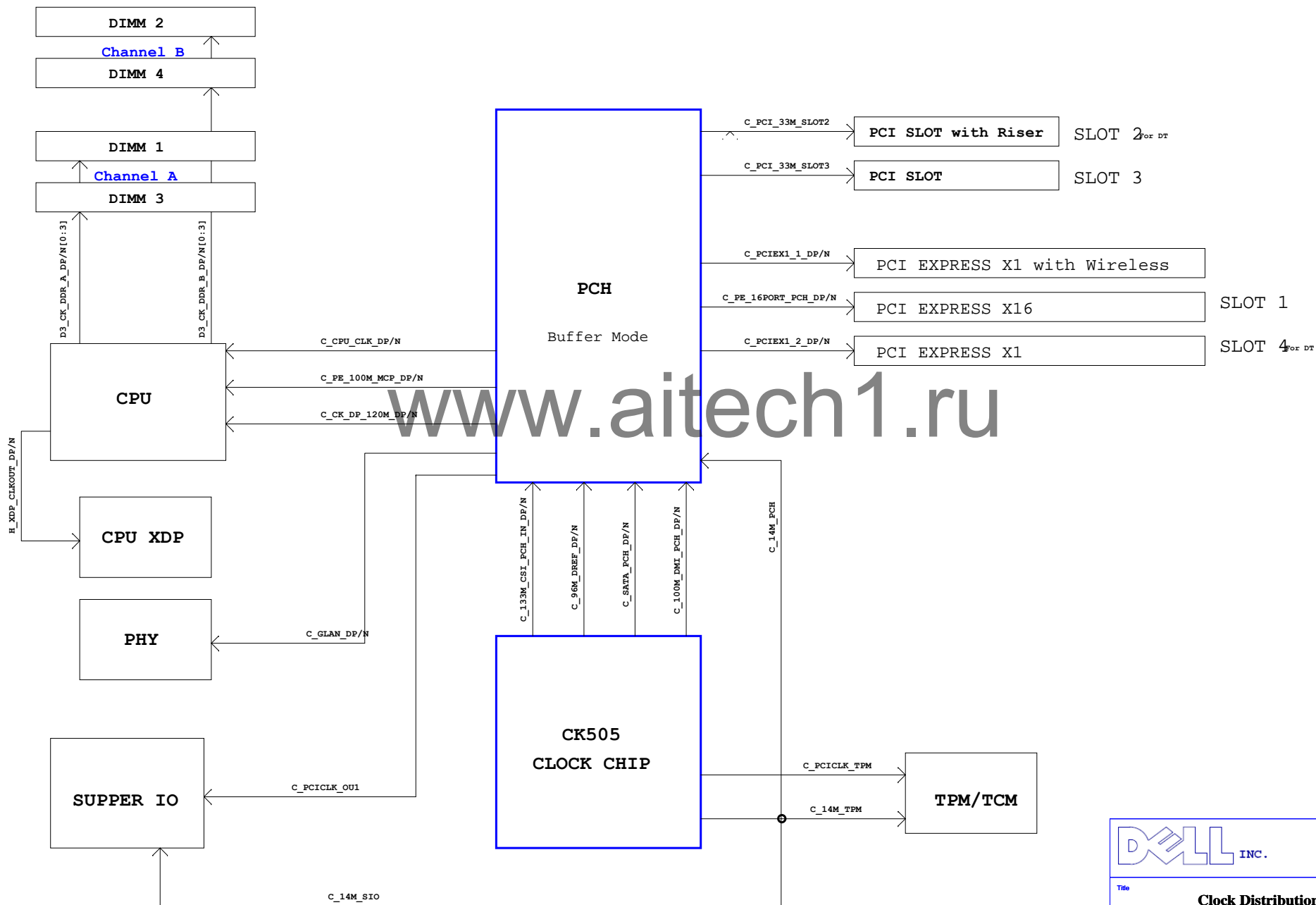
DESIGN	CHECK	APPROVE
Hiko Pan Ronie Ko	Ivan	Ping-kun

DELL INC.	
Cover Sheet	
Title	
DWG NO	Rev
Wembley_MT	
Date: Wednesday, April 14, 2010	Sheet 1 of 61

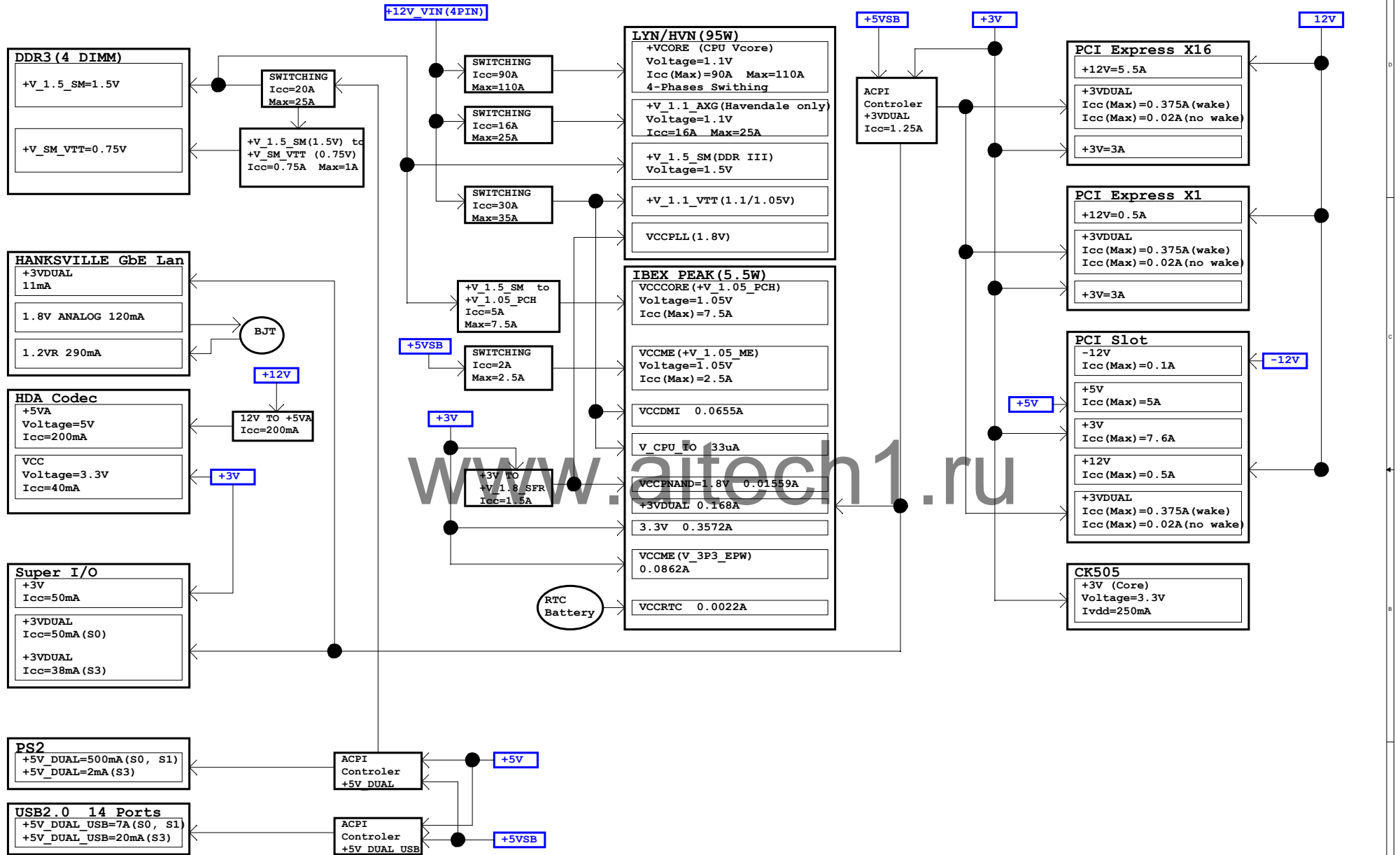
SMBUS DIAGRAM



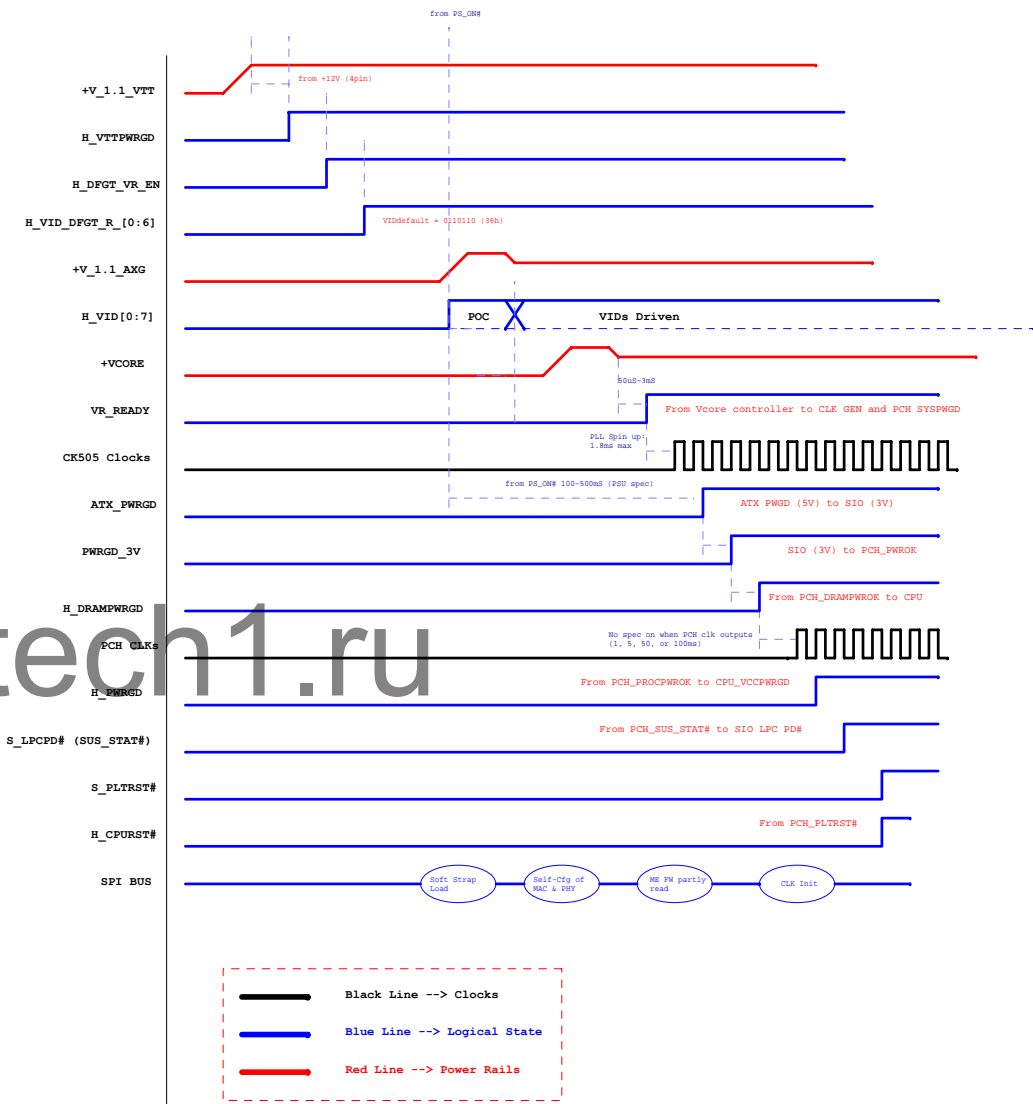
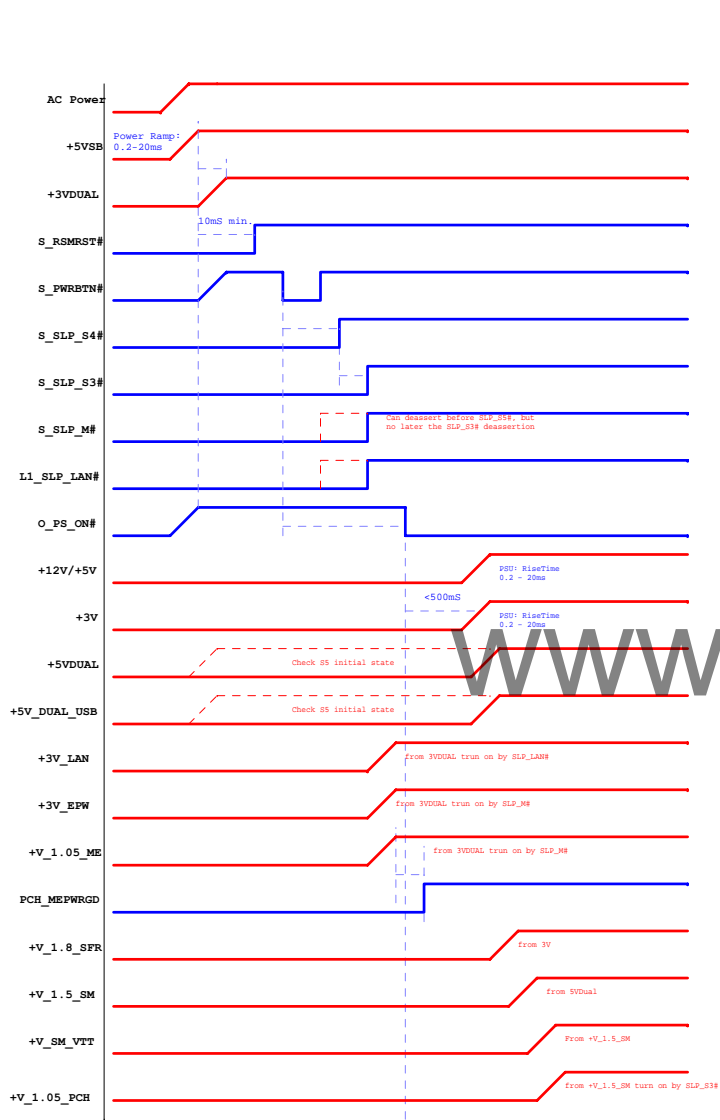
CLOCK DISTRIBUTION



POWER DELIVERY MAP



POWER ON SEQUENCE

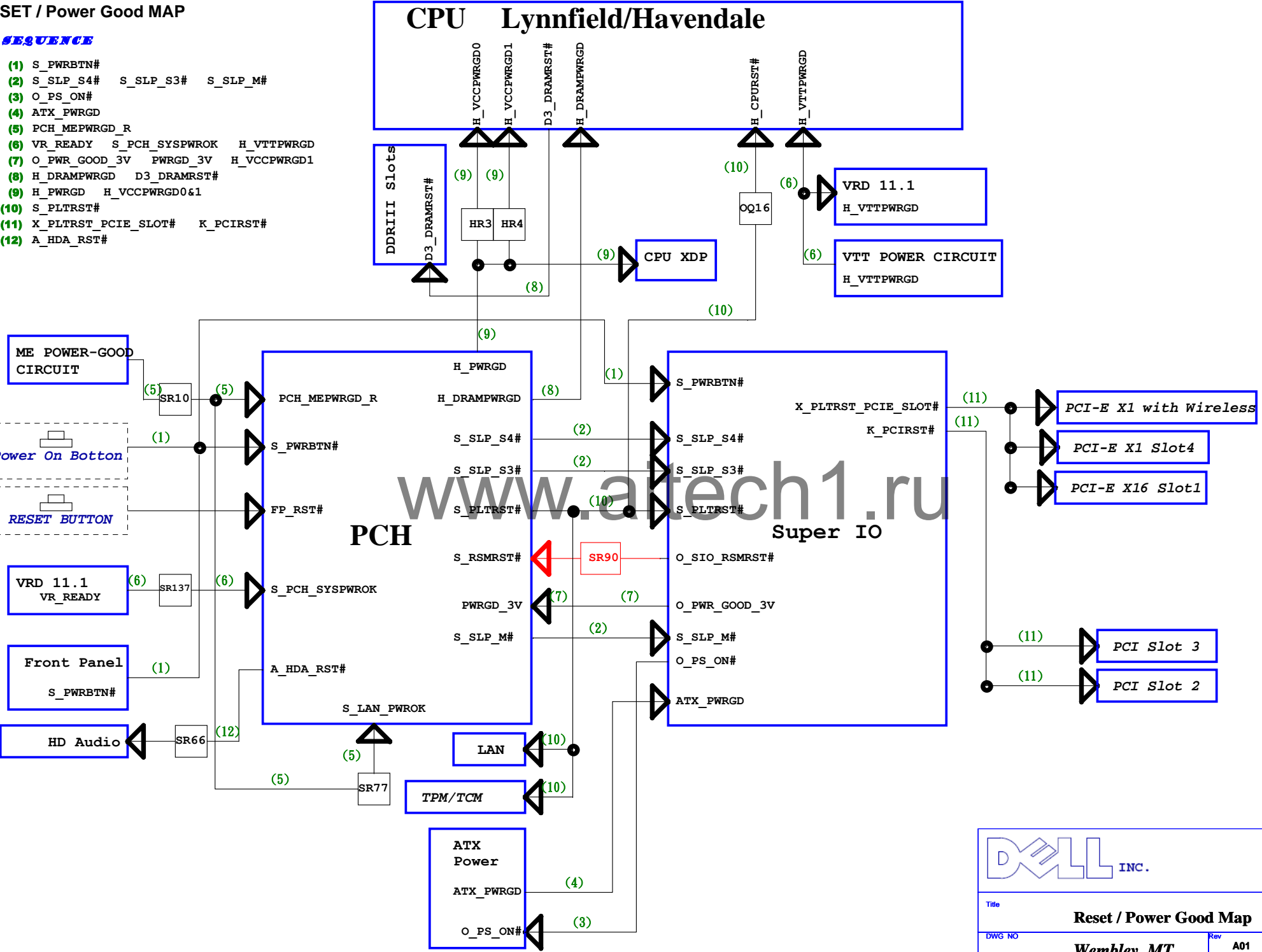


RESET / Power Good MAP

CPU Lynnfield/Havendale

SEQUENCE

- (1) S_PWRBTN#
- (2) S_SLP_S4# S_SLP_S3# S_SLP_M#
- (3) O_PS_ON#
- (4) ATX_PWRGD
- (5) PCH_MEPWRGD_R
- (6) VR_READY S_PCH_SYSPWROK H_VTTPWRGD
- (7) O_PWR_GOOD_3V PWRGD_3V H_VCCPWRGD1
- (8) H_DRAMPWRGD D3_DRAMRST#
- (9) H_PWRGD H_VCCPWRGD0&1
- (10) S_PLTRST#
- (11) X_PLTRST_PCIE_SLOT# K_PCIRST#
- (12) A_HDA_RST#



IRQ Routing Table

	INTA#	INTB#	INTC#	INTD#	IDSEL	REQn#	GNTn#
Slot2	A	B	C	D	16	0	0
Slot3	C	D	A	B	18	2	2
Riser	B	C	D	A	17	1	1

STRAPPING Table

CPU side

H_CPU_CFG	H	L	Description
0	See PEG Config Table		PEG SEL0
1			PEG SEL1
2			PEG SEL2
3	Normal	Reversed	LANE Reversal Default
4	Disable	Enable	DP Presence Default
5	RSVD		
6	RSVD		
7	RSVD		
15	RSVD		

PEG Config Table

PEG SEL2	PEG SEL1	PEG SEL0	PEG Config
1	1	1	1 X 16 Default
1	1	0	2 X 8

Clock Gen.

FREQ	C_CK_BSEL0	C_CK_BSEL0	C_CK_BSEL0
100	1	0	1
133	1	0	0 Default

PIN NAME	NET		Strapping description
PCI2/TME (PIN4)	CK_PIN4	1	Overclocking DISABLED DEFAULT
		0	Overclocking ENABLED
PCI3/CFG (PIN5)	CK_PIN5	1	CGF TABLE ENABLED
		0	CGF TABLE DISABLED DEFAULT
PCI4/SRC5_EN (PIN6)	CK_PIN6	1	SRC5 DEFAULT
		0	CPU_STOP# and PCI_STOP#
PCI_F5/ITP_EN (PIN7)	CK_PIN7	1	CPU_ITP
		0	SRC8 DEFAULT

SIO SMSC5544 Functional Straps

PIN NAME	NET		Strapping description
GP070 / PWM4 (PIN127)	O_SPEAKER	1	Diag_En Disable
		0	Diag_En Enable DEFAULT
DTR1# [TEST_EN] /GP051 (PIN104)	O_DTR1#	1	PE BOOT Loader Strap (DTR1#)= Load from SPI
		0	PE BOOT Loader Strap (DTR1#)= No Load from SPI DEFAULT

On-Die PLL Voltage Regulator Voltage Select

HAD_SYNC	Description
High	1.5V
Low	1.8V DEFAULT

On-Die PLL Voltage Regulator

GPI027	Description
High	Regulator is enabled. DEFAULT
Low	Regulator is disabled.

Topblock swap mode

GNT3# (Internal pull up)	Description
High	Topblock swap mode: Disable DEFAULT
Low	Topblock swap mode: Enable

No reboot mode

SPKR (Internal pull down)	Description
High	No reboot mode: Enable
Low	No reboot mode: Disable DEFAULT

Integrated 1.1V VRM

INTVRMEN	Description
High	Integrated 1.1V VRM: Enable DEFAULT
Low	Integrated 1.1V VRM: Disable

Intel Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable

S_NVR_ALE	Description
High	Anti-Theft Technology: Enable DEFAULT
Low	Anti-Theft Technology: Disable

Intel Management Engine features (S_MFG_MODE#)

GPI033	Description
High	Intel Management Engine: Enable DEFAULT
Low	Intel Management Engine: Disable

TPM Functionality

SPI_MOSI (Internal pull down)	Description
High	TPM Functionality: Enable
Low	TPM Functionality: Disable DEFAULT


DMI termination voltage

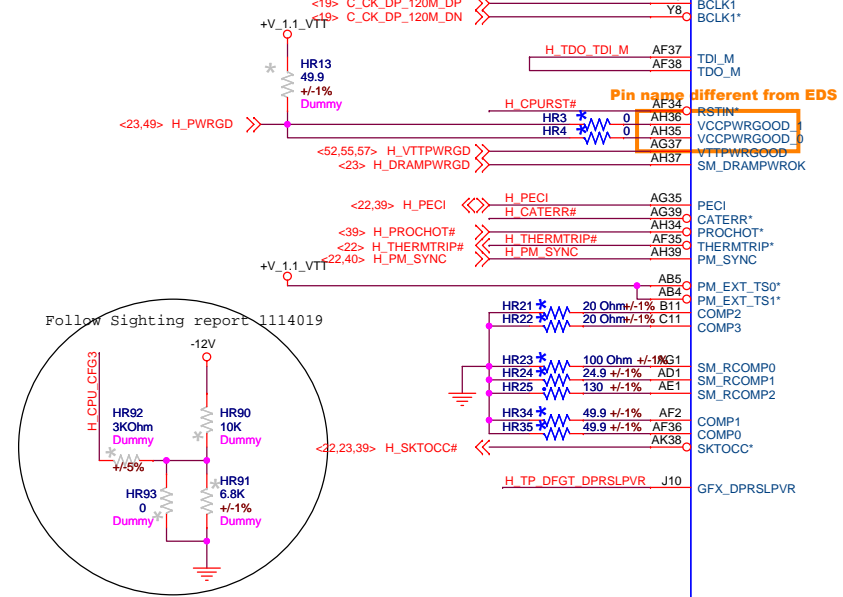
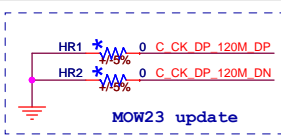
NV_CLE (Internal pull down)	Description
High	DMI termination voltage : Enable
Low	DMI termination voltage : Disable DEFAULT

Boot BIOS Destination Selection

GNT1# (Internal pull up)	GNT0# (Internal pull up)	Description
Low	High	Reserved
High	Low	Flash cycle routed to PCI
High	High	Flash cycle routed to SPI DEFAULT
Low	Low	Flash cycle routed to LPC

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GPIO/IRQ/IDSEL Table	
Title DWG NO Wembley_MT	Rev A01
Date: Wednesday, April 14, 2010 Sheet 7 of 61	



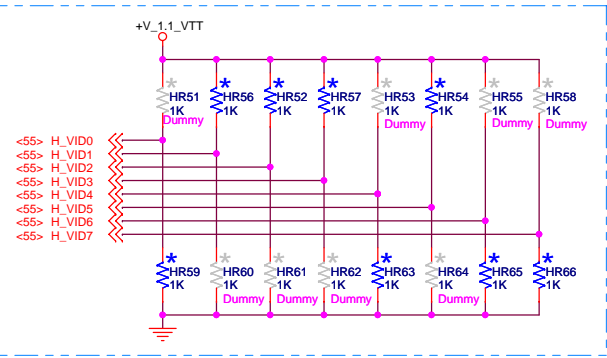
CFG7 placing a 3.01K +/- 5% pull down resistor to VSS on LGA1156 processor signal CFG[7] (land F9). This pull down resistor should be removed when this issue is fixed.

CFG Table			
CFG	H / L	Description	
0	PEG Config Table	PEG SEL0	
1	PEG Config Table	PEG SEL1	
2	PEG Config Table	PEG SEL2	
3	Normal / Reverse	Lane Reverse	
4	Disable / Enable	DP Presence	
5		RESERVED	
6		RESERVED	
7		RESERVED	
15		RESERVED	

CFG[0..5] HAVE INTERNAL PULL-UP			
PEG Config Table			
SEL2	SEL1	SEL0	PCI-E Config
1	1	1	1 x 16
1	1	0	2 x 8

9/18: as CRB 1.0

Power On Config		
	Function	Default
VID0	MSI0	0
VID1	MSI1	1
VID2	MSI2	1
VID3	IMON CONFIG0	1
VID4	IMON CONFIG1	0
VID5	IMON CONFIG2	1
VID6	RESERVED	
VID7	VRD SELECT	Low
PSI#	RESERVED	Low



- VID0/MSID0

VID1/MSID1

VID2/MSID2

VID3/MSID3

VID4/MSID4

VID5/MSID5

VID6/MSID6

VID7/MSID7

PSI#

GFX_VR_EN

GFX_IMON

GFX_VID0

GFX_VID1

GFX_VID2

GFX_VID3

GFX_VID4

GFX_VID5

GFX_VID6

FC_AE38

VTT_SELECT

FC_AG40

VCC_SENSE

VSS_SENSE

VTT_SENSE

VSS_SENSE_VTT

VAXG_SENSE

VSSAXG_SENSE

ISENSE

TDO

TDI

TCK

TMS

TRST#

PRDY#

PRB#

BCLK_TPD

BCLK_TTP

TAPPWRGOOD

RESET_OBS#

BPM0#

BPM1#

BPM2#

BPM3#

BPM4#

BPM5#

BPM6#

BPM7#
- U40

U38

U37

U36

U35

U34

U33

AG38

F12

F6

G10

B12

E12

E11

G11

J11

AE38

AF39

AG40

T35

T34

AE35

AE36

A13

B13

T40

AM38

AM37

AN37

AN40

AM39

AJ38

AK37

AL40

AK40

AK39

AK34

AL39

AL33

AL32

AK33

AK32

AM31

AL30

AK30

AK31
- H_VID0

H_VID1

H_VID2

H_VID3

H_VID4

H_VID5

H_VID6

H_VID7

H_MCP_PSI#

H_DFGT_VR_EN

H_VID_DFGT_R_0

H_VID_DFGT_R_1

H_VID_DFGT_R_2

H_VID_DFGT_R_3

H_VID_DFGT_R_4

H_VID_DFGT_R_5

H_VID_DFGT_R_6

H_VTT_VID1

H_VCC_SENSE

H_VSS_SENSE

H_VCCITT_SENSE

H_VSSITT_SENSE

H_VCCAGX_SENSE

H_VSSAGX_SENSE

H_MCP_ISENSE_DP

H_TDO

H_TDI

H_TCK

H_TMS

H_TRST#

H_PRDY#

H_PRB#

H_XDP_CLKOUT_DN

H_XDP_CLKOUT_DP

H_TAPPWRGOOD

H_RSTOUT#

H_TP_MCP_BPM0

H_TP_MCP_BPM1

H_TP_MCP_BPM2

H_TP_MCP_BPM3

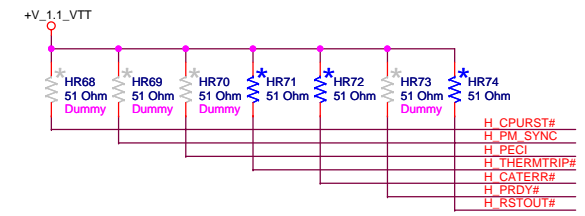
H_TP_MCP_BPM4

H_TP_MCP_BPM5

H_TP_MCP_BPM6

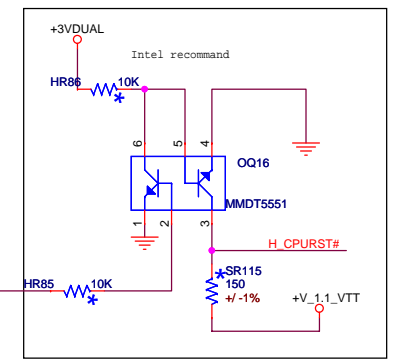
H_TP_MCP_BPM7

Test pin



Signal	DG 0.8	CRB 1.0
H_RSTOUT#	Pull-High to Vtt	Pull-High to Vtt
H_PRDY#	Pull-High to Vtt	Floating
H_CATERR#	Pull-High to Vtt	Pull-High to Vtt
H_THERMTRIP#	Pull-High to Vtt	Pull-High to Vtt
H_PECI	Pull-High to Vtt	Floating
H_CPURST#	Pull-High to Vtt	Pull-High to Vtt
H_PM_SYNC	Pull-High to Vtt	Floating

All resistors are 51.1ohm



Processor Icc(max)	I _{MAX} Iout gain: 900 mV = I _{MAX}	POC Gain Setting
Disabled	-	000
Icc(max) ≤ 40 A	40 A	001
40 A < Icc(max) ≤ 60 A	60 A	010
60 A < Icc(max) ≤ 80 A	80 A	011
80 A < Icc(max) ≤ 100 A	100 A	100
100 A < Icc(max) ≤ 120 A	120 A	101
120 A < Icc(max) ≤ 140 A	140 A	110
140 A < Icc(max) ≤ 180 A	180 A	111

CPU-1:MISC

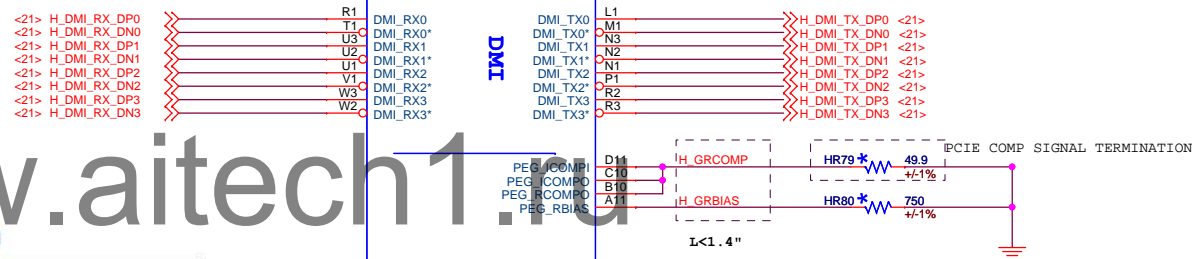
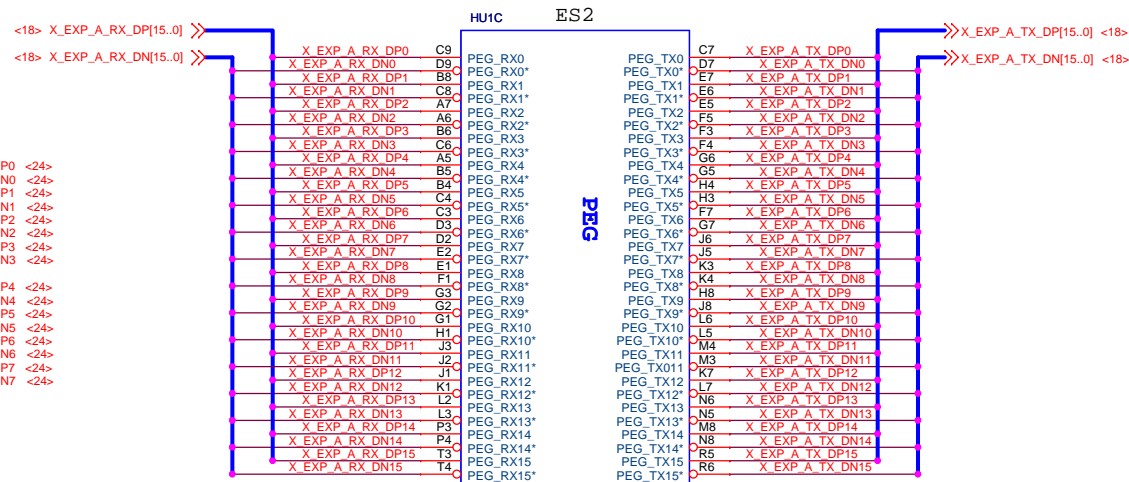
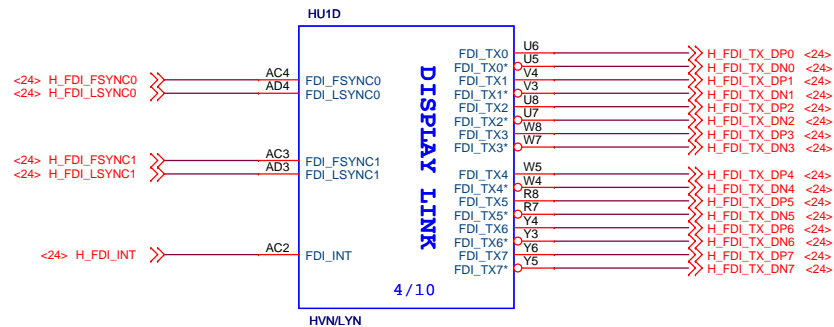
Wembley_MT

Rev

A01

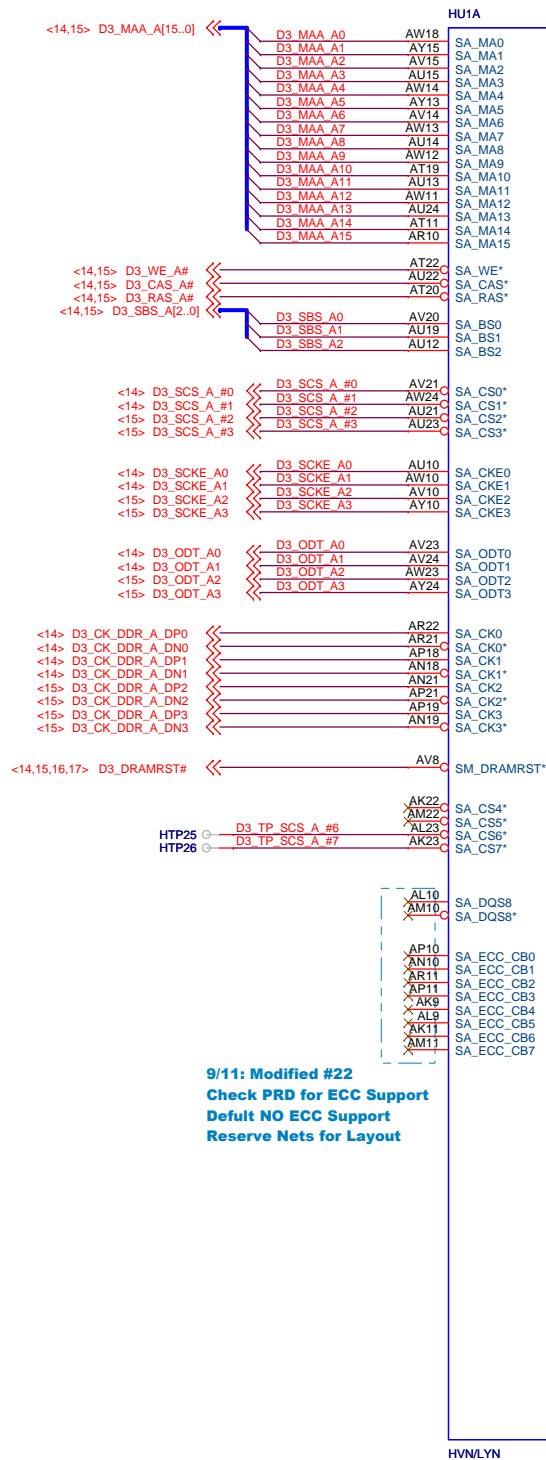
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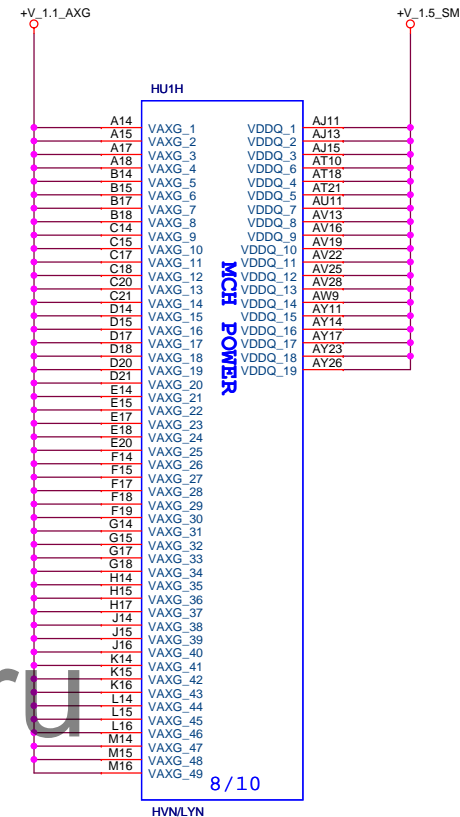
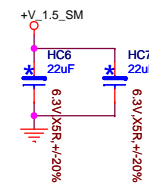
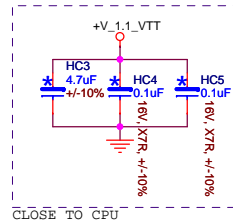
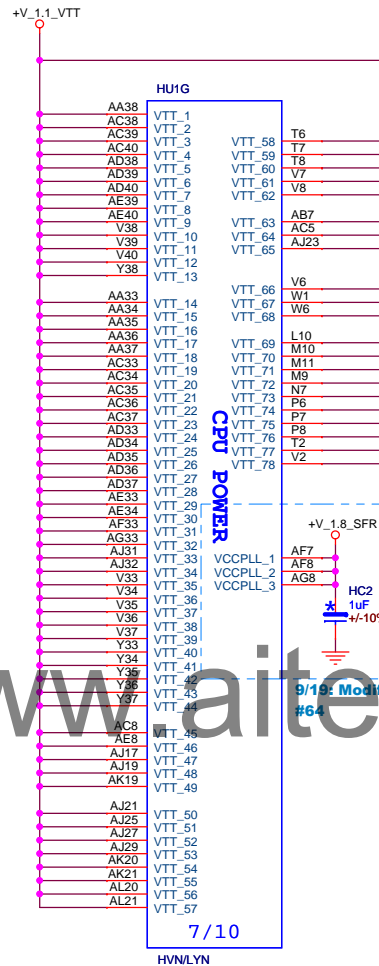
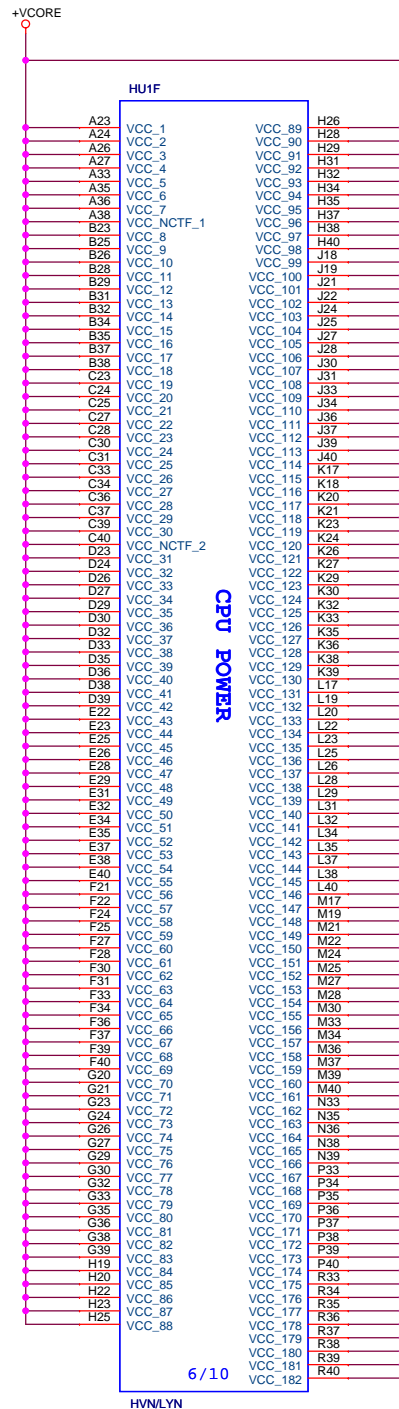
Sheet 8 of 61



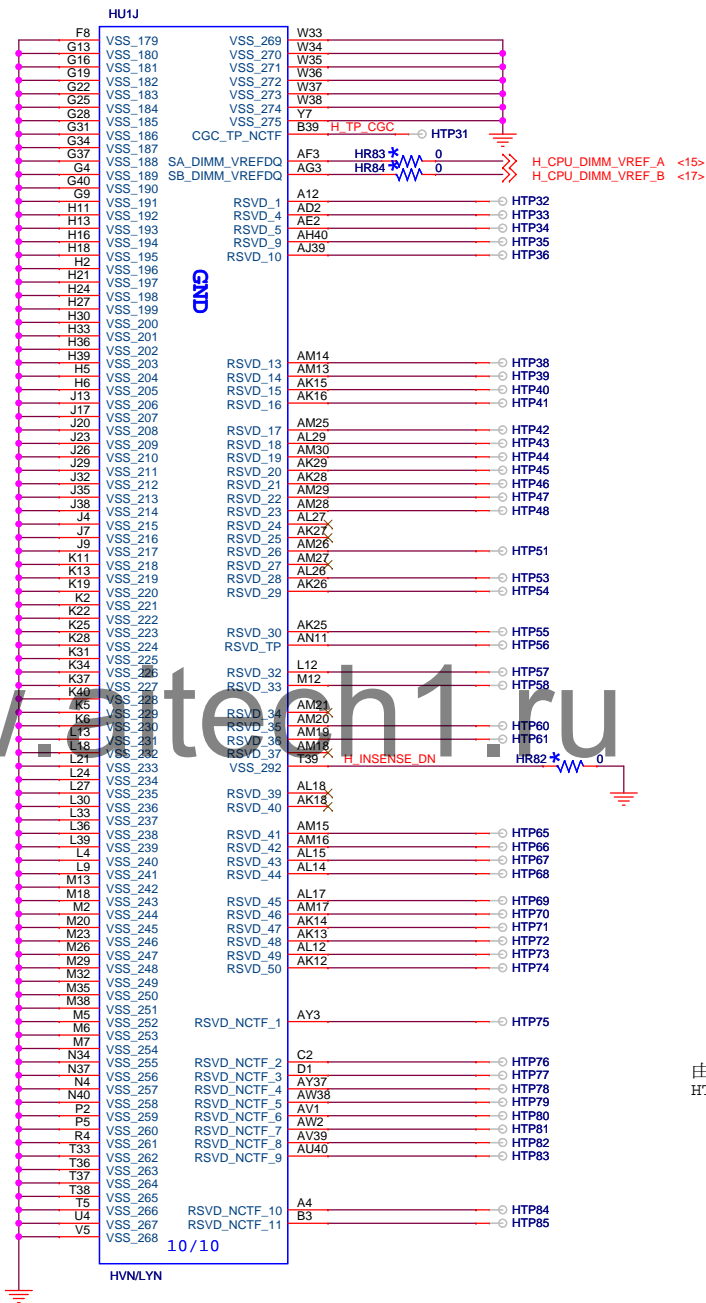
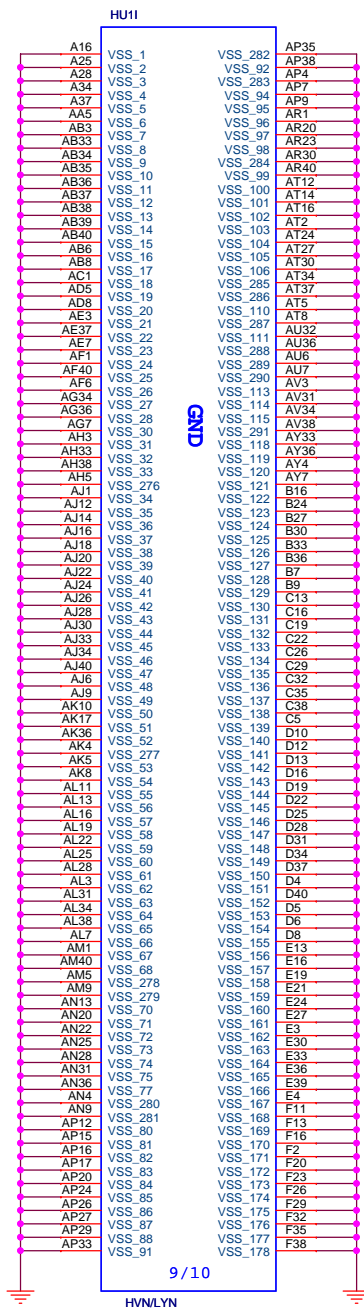
Signals Not Used by the Lynnfield Processor, Listed by Platform

Platform	Interface	Signals Not Used ¹
Desktop, Server and Workstation Ixex Peak Platforms	Intel Flexible Display Interface	FDI_FSYNC[1:0]
		FDI_LSYNC[1:0]
		FDI_INT
		FDI_TX[7:0]
		FDI_TX#[7:0]
	Integrated Graphics Core Power	GFX_DPRSLPVR
		GFX_IMON
		GFX_VID[6:0]
		GFX_VR_EN
		VAXG
Desktop Ixex Peak Platforms	Memory	SA_DM[7:0]
	Other	SB_DM[7:0]
		VCCPWRGOOD_1
		SA_CS#[7:4]
Desktop Ixex Peak Platforms	Memory Interface: RDIMM Related	SB_CS#[7:4]





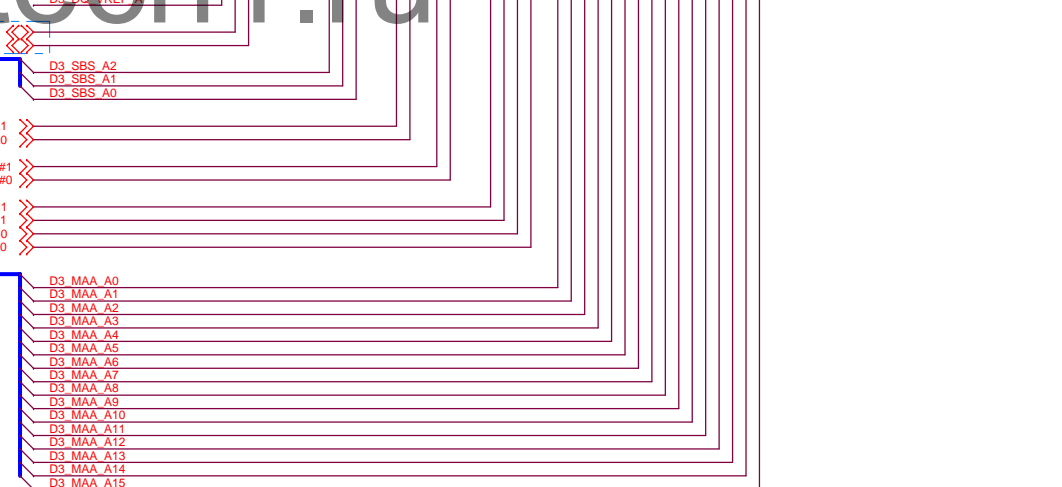
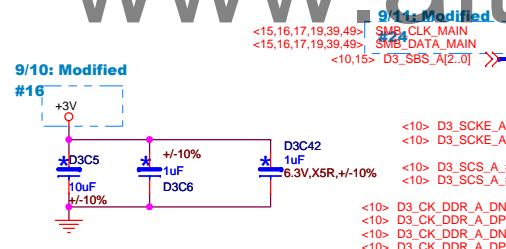
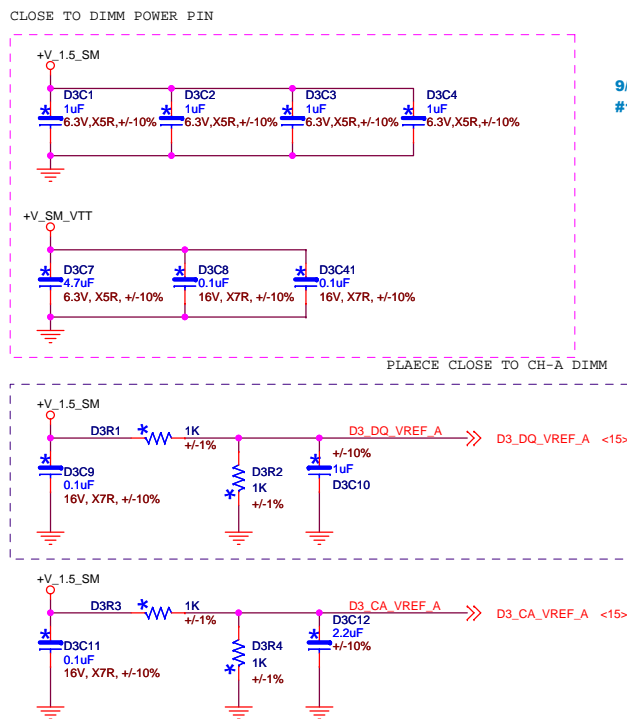
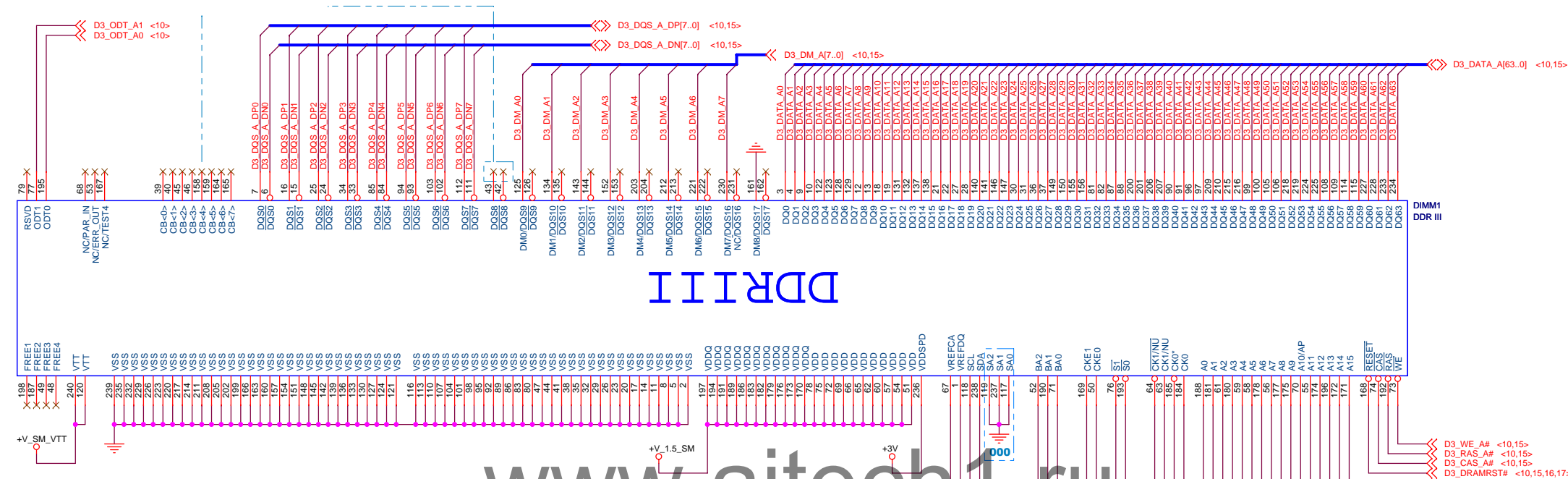
DELL INC.	
CPU-6:POWER	
DWG NO	Rev
Wembley_MT	
Date: Wednesday, April 14, 2010	Sheet 12 of 61



由于Power要follow CRB 下述测试点不能加上：
HTP59, HTP50, HTP52, HTP28, HTP49, HTP62, HTP23, HTP64, HTP63

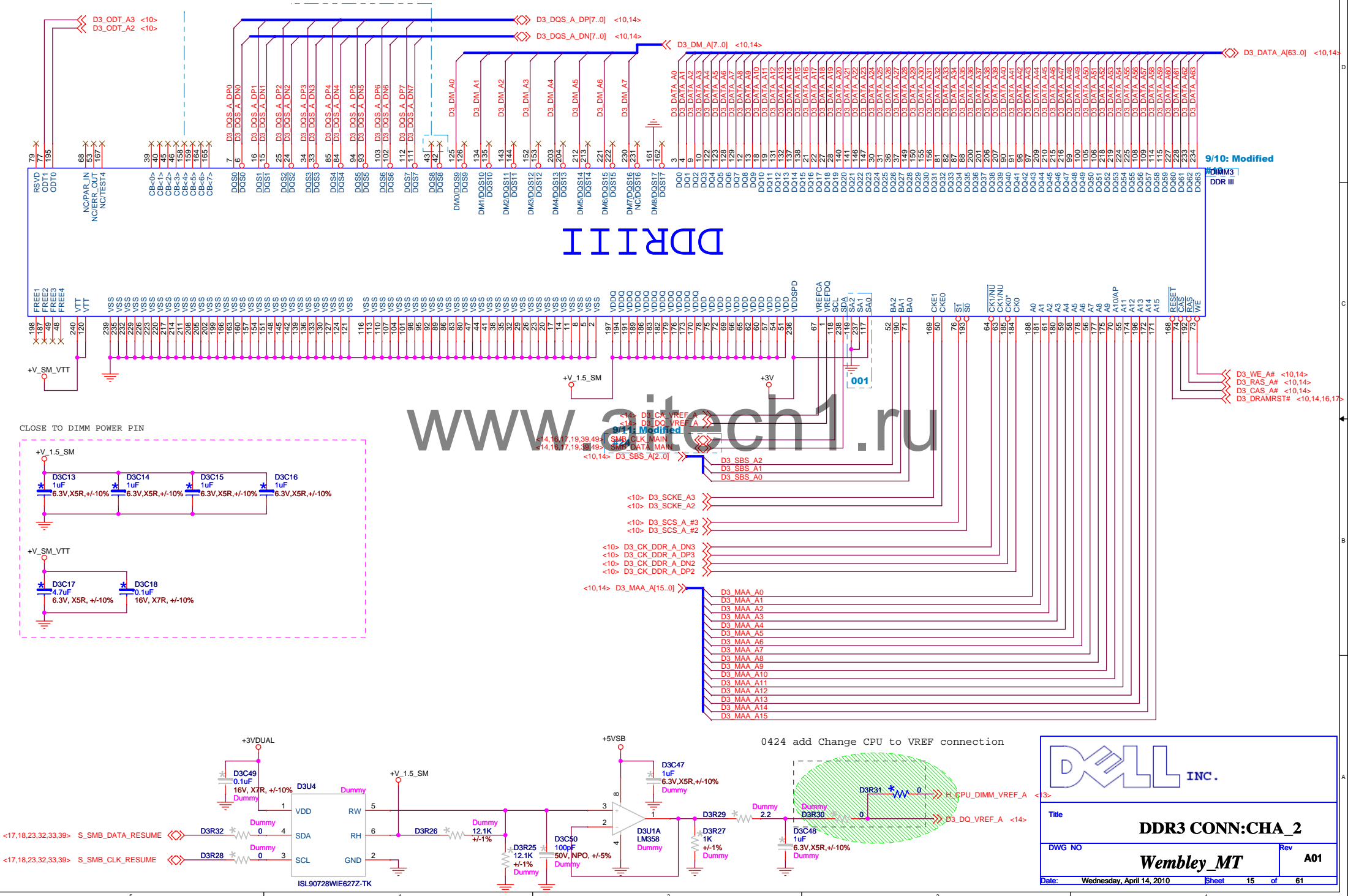
		Title	
		CPU-7:GND	
DWG NO	Rev		A01
Wembley_MT			
Date: Wednesday, April 14, 2010	Sheet	13	of 61

CHANNEL A BANK 1
SMB ADDRESS:000

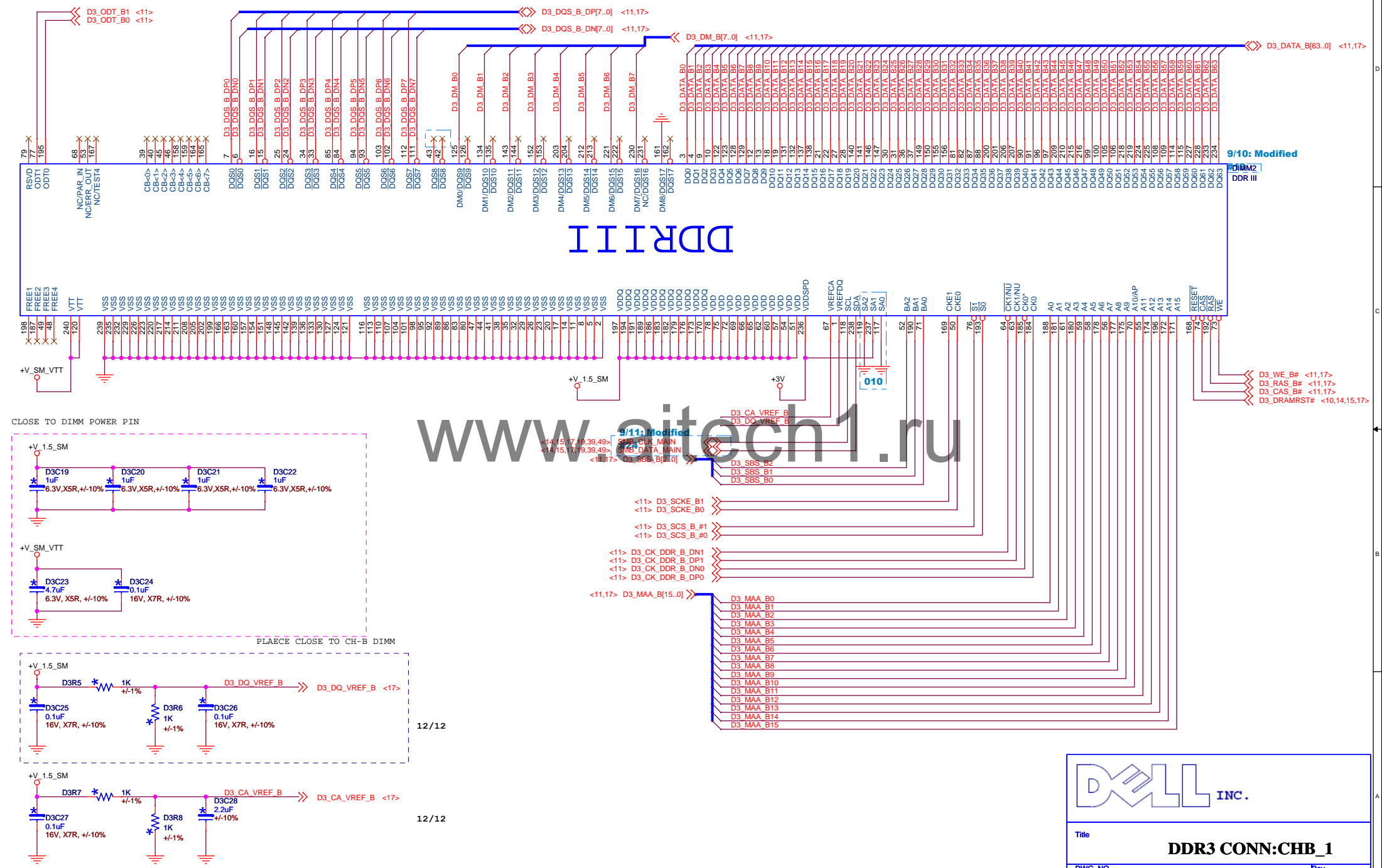


Title		DDR3 CONN:CHA_1	
DWG NO		Rev	
<i>Wembley_MT</i>		A01	
Date:	Wednesday, April 14, 2010	Sheet	14 of 61

CHANNEL A BANK 2
SMB ADDRESS:001



CHANNEL B BANK 1
SMB ADDRESS:010



Title

DDR3 CONN:CHB_1

DWG NO

Wembley_MT

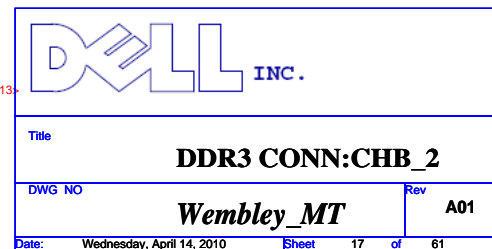
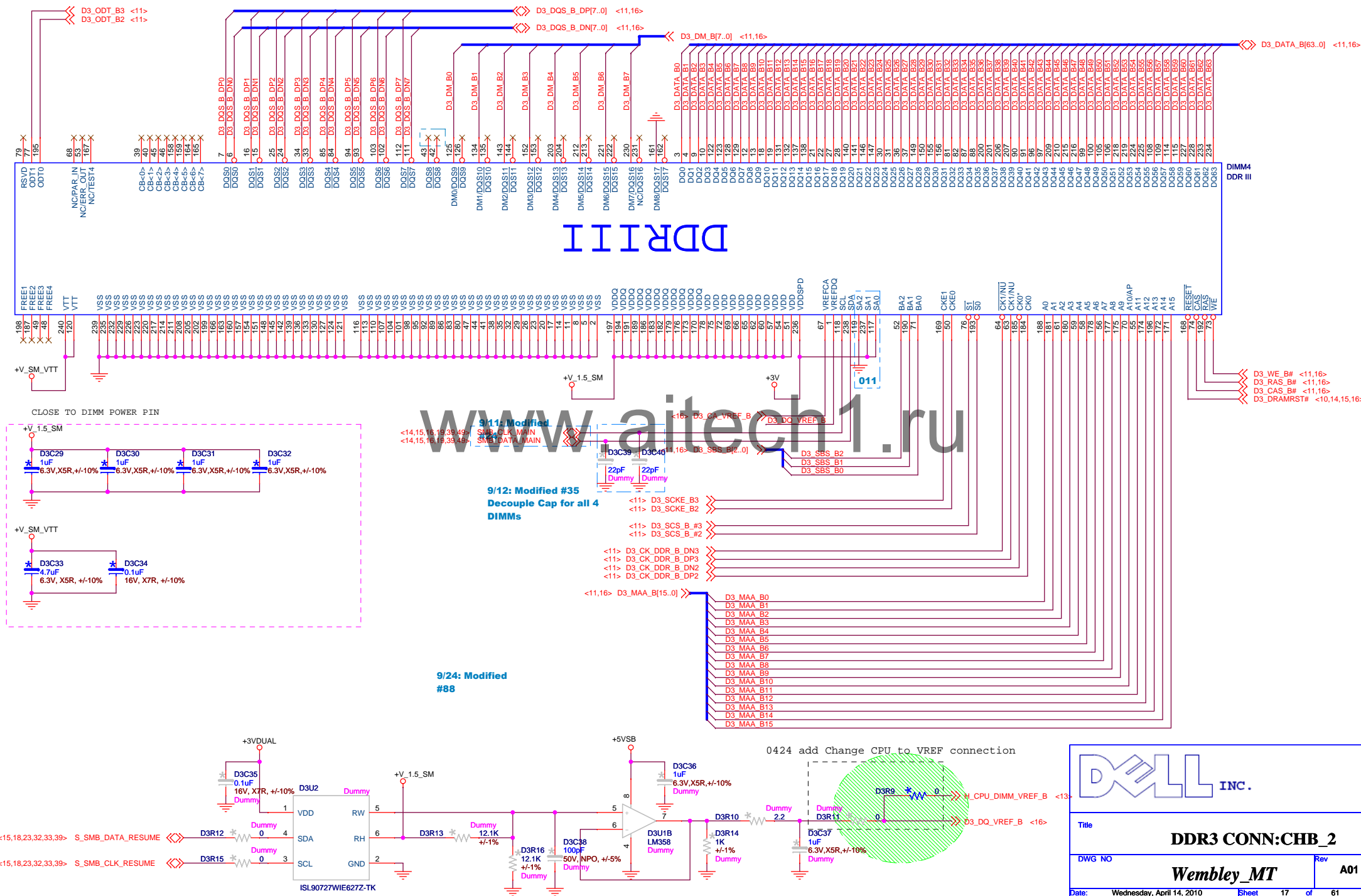
Date: Wednesday, April 14, 2010

Sheet 16 of 61

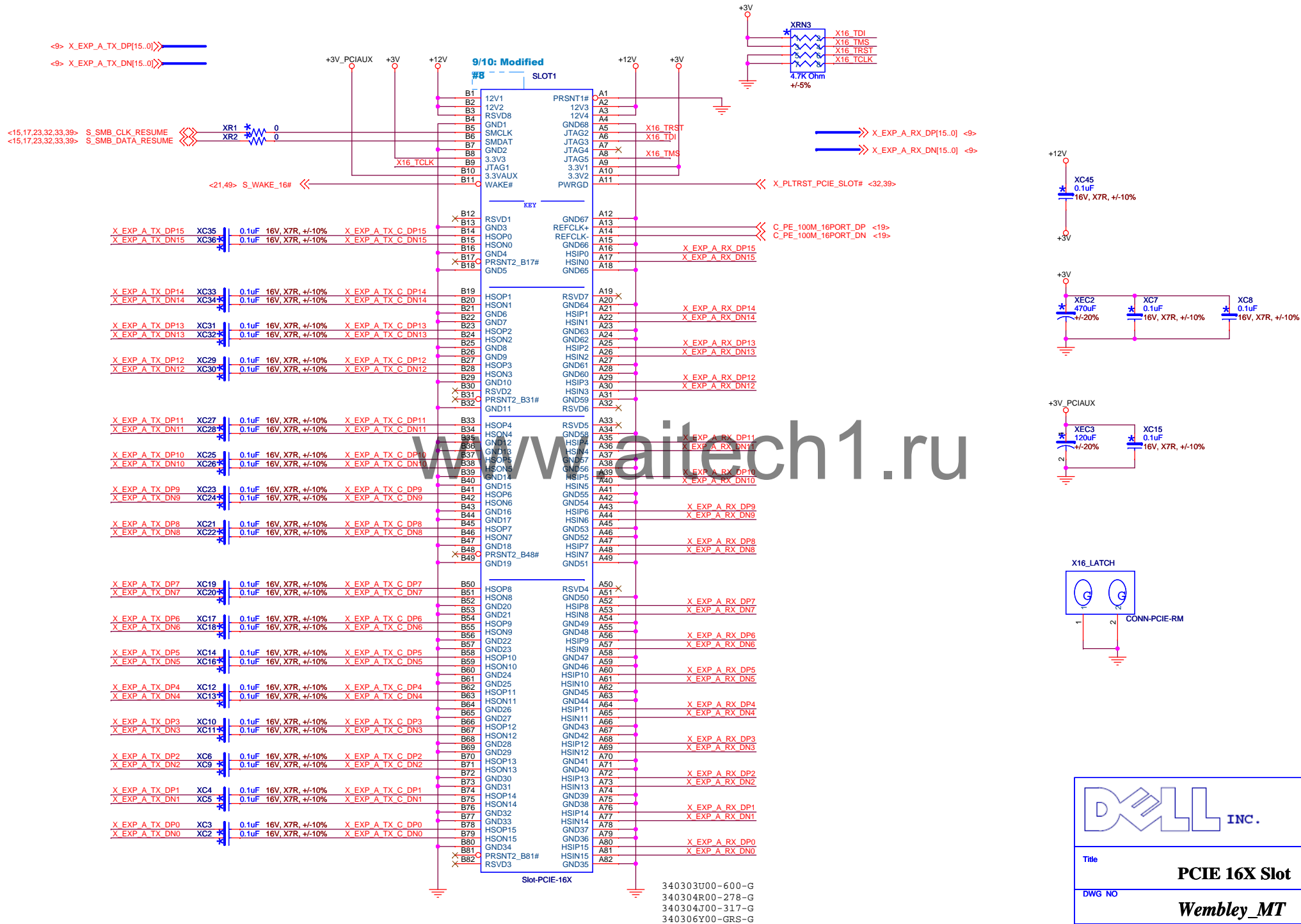
Rev


A01

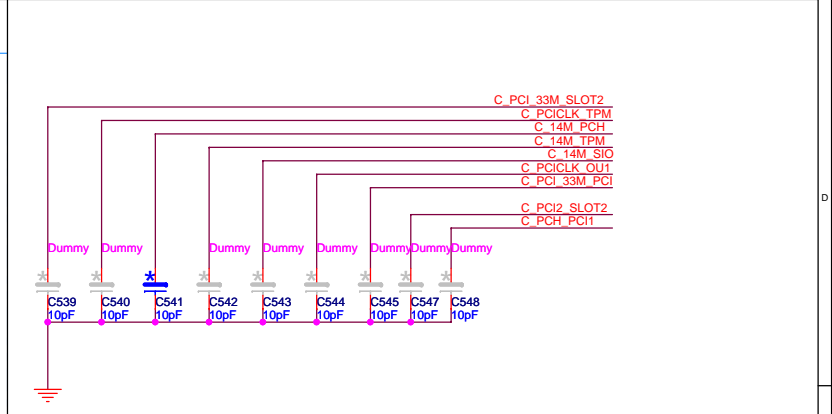
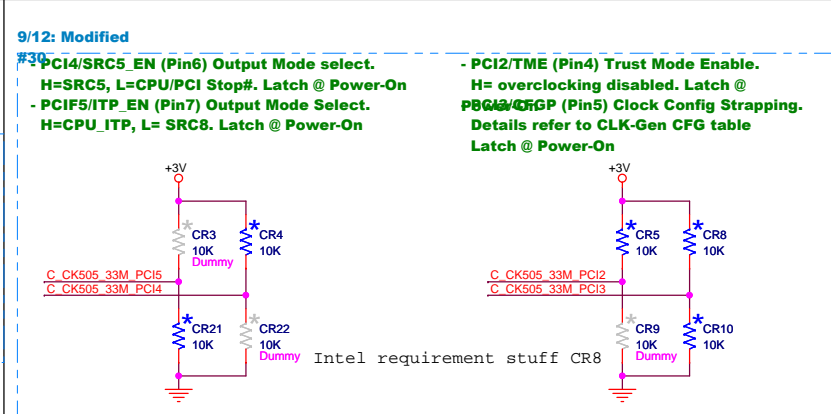
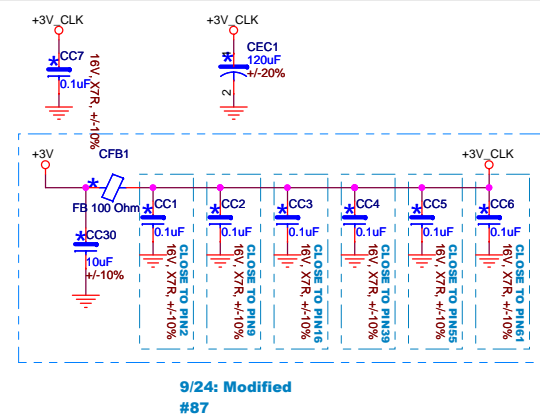
CHANNEL B BANK 2
SMB ADDRESS:011



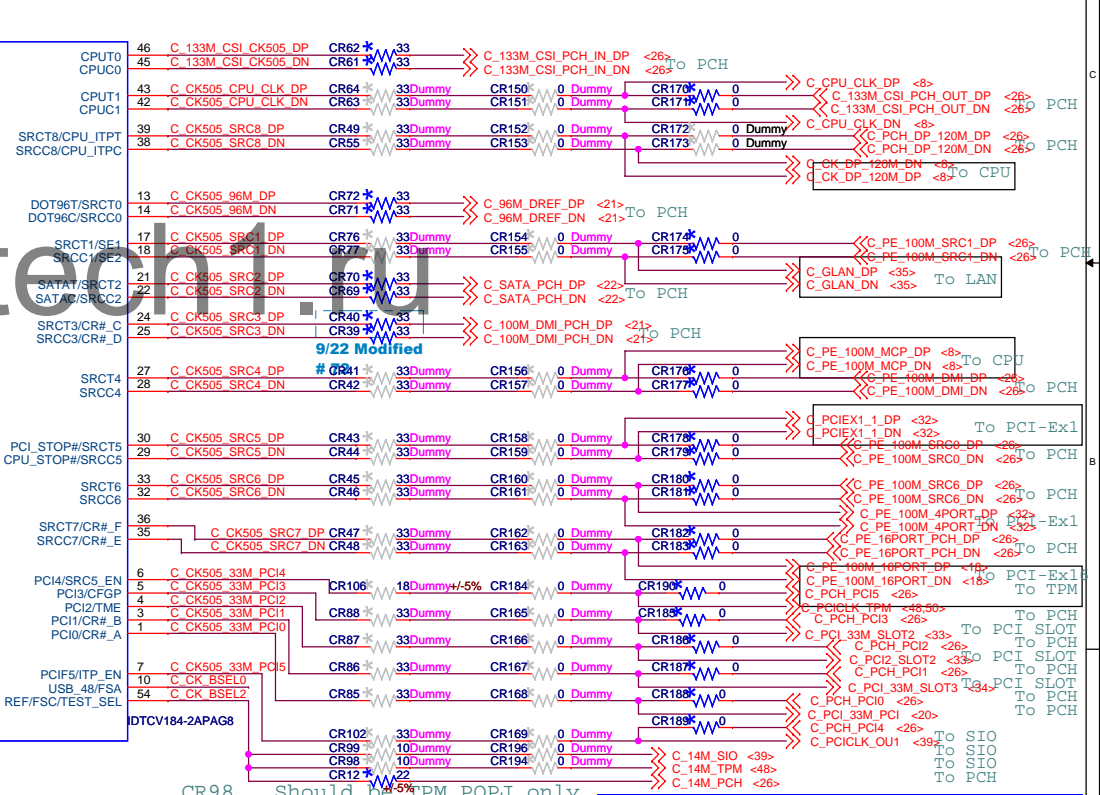
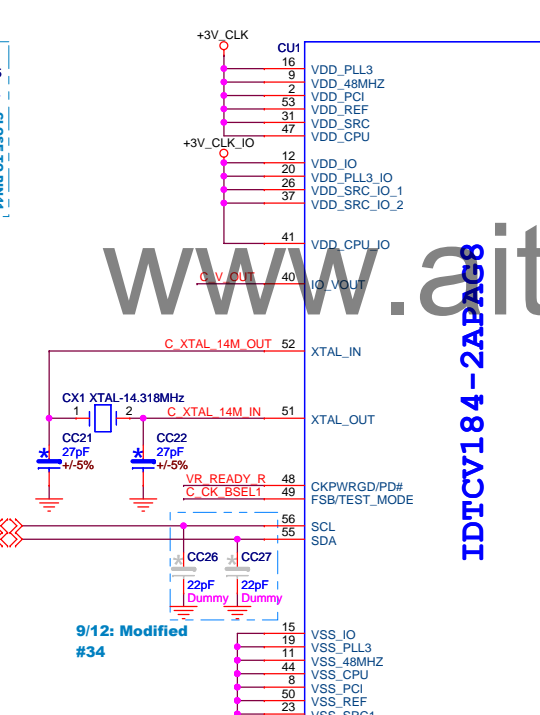
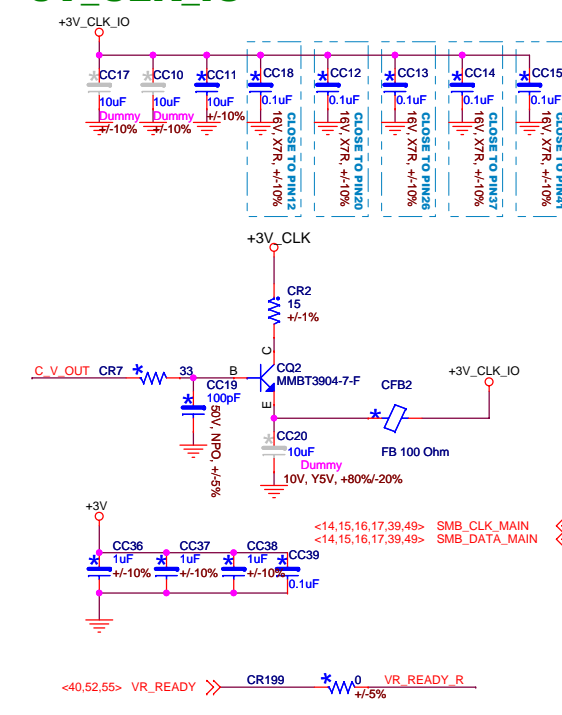
PCIEX16



 INC.		PCIE 16X Slot	
		DWG NO	Rev
Wembley_MT		A01	
Date:	Wednesday, April 14, 2010	Sheet	18 of 61

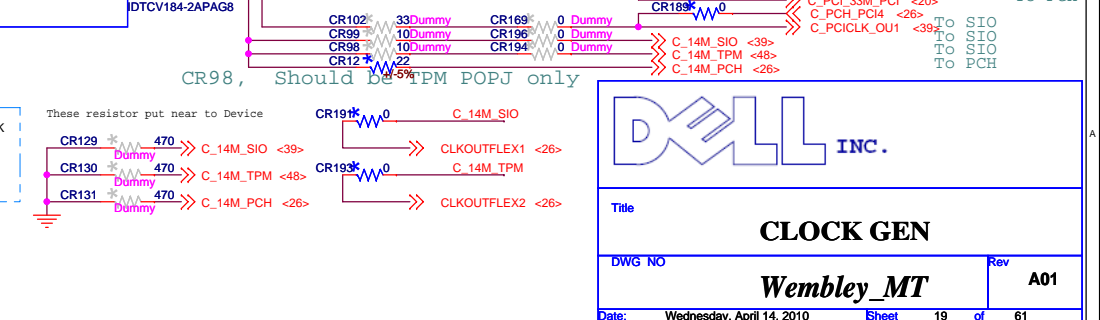
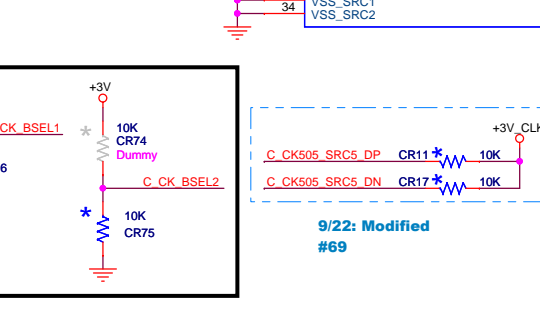


+3V_CLK_IO



9/11: Modified #27
check sequencing of CLK & Vcore, once DG come out

FREQ	BSEL0	BSEL1	BSEL2
100	1	0	1
133	1	0	0

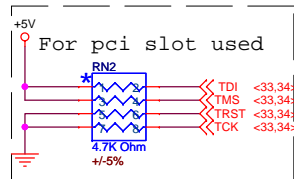


INC.

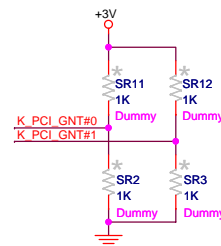
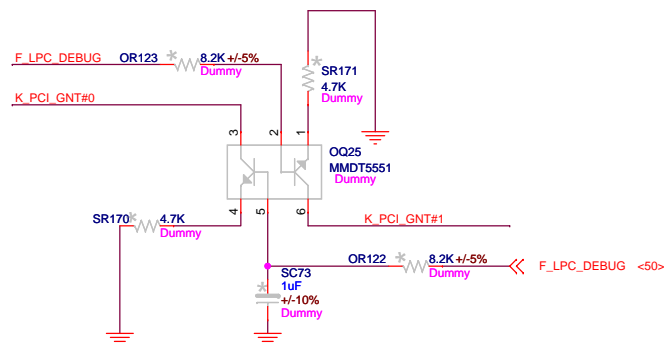
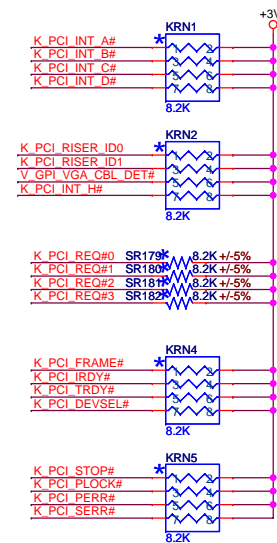
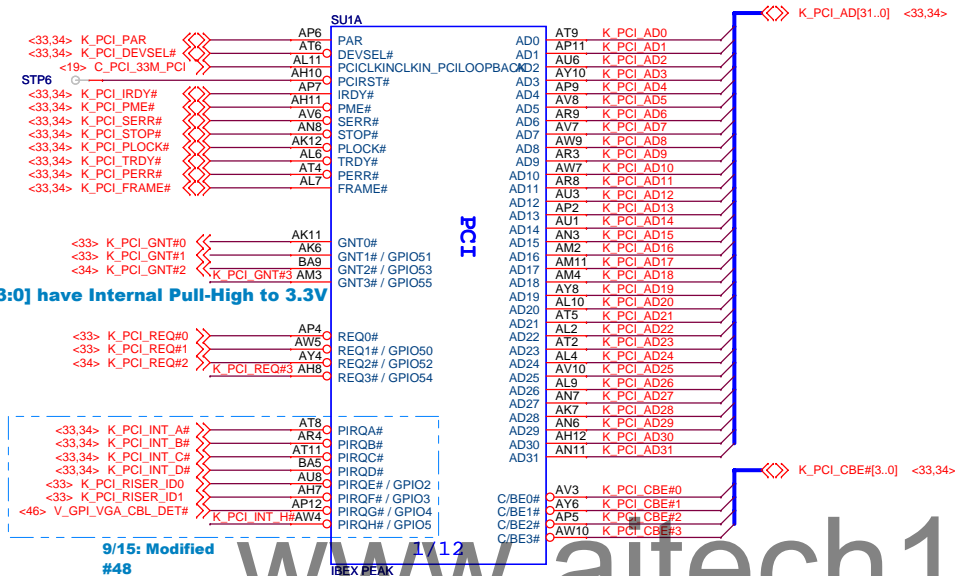
CLOCK GEN

DWG NO **Wembley_MT**

Date: Wednesday, April 14, 2010 Sheet 19 of 61



GNT [3:0] have Internal Pull-High to 3.3V



Boot BIOS Select

Boot Device	GNT1	GNT0
LPC	0	0
PCI	1	0
Reserved	0	1
SPI	1	1

EDS 1.0 / DG 0.8

GNT2 configures DMI for ESI compatible mode is for server platforms only

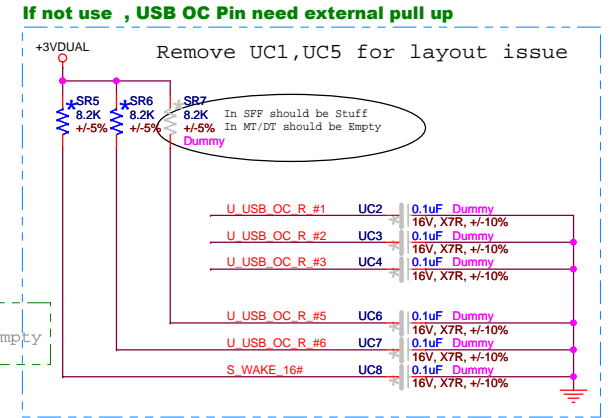
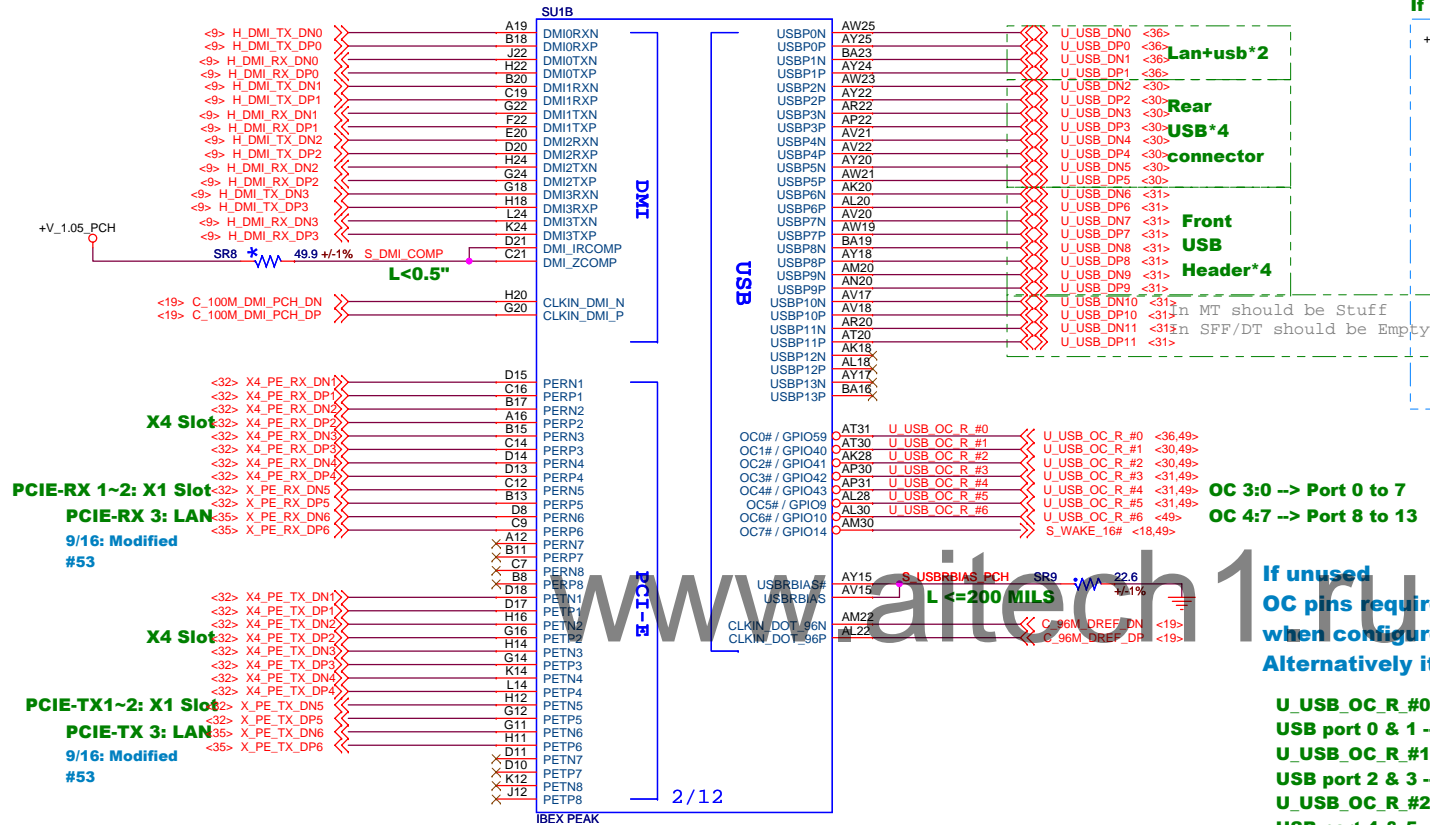


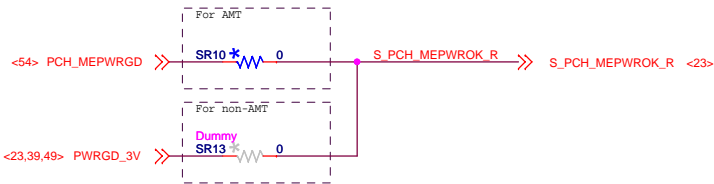
GNT3# Internal pull-up.

EDS 1.0 / DG 0.8

GNT3 is Swap OverRide Strap OverRide if sample Low

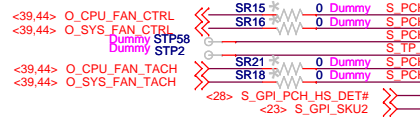




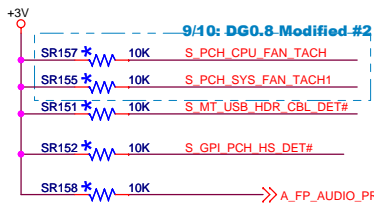
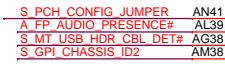


STEVEN UPDATE 08/09/01

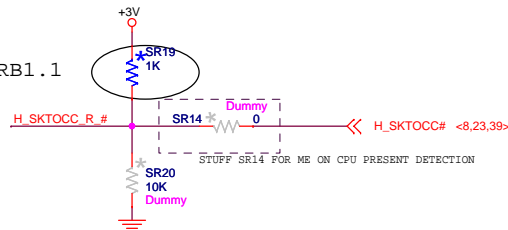
Place close to FAN conn



SMSC 5524 doesn't support SST



Follow CRB1.1



CINK

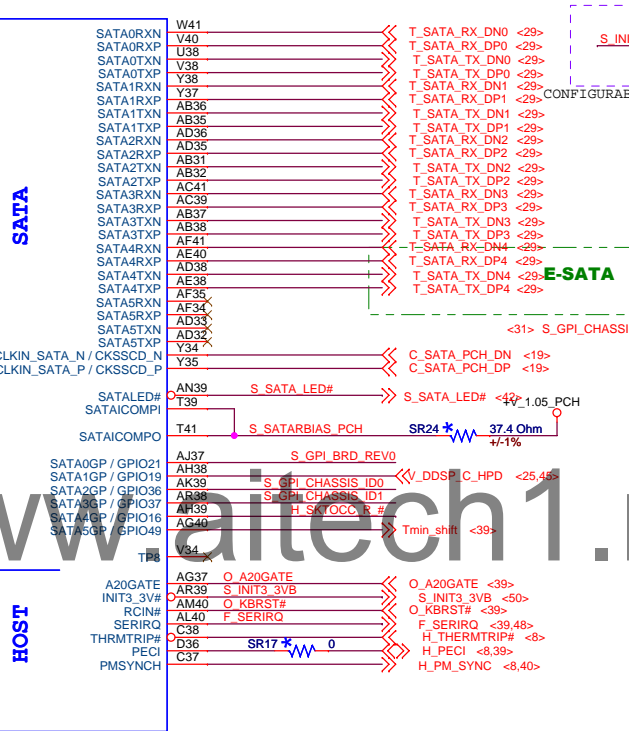
FAN

GPIO

HOST

3/12

IBEX PEAK



CONFIGURABLE CPU OUTPUT STRONGER IF LOW

E-SATA

<31> S_GPI_CHASSIS_ID2

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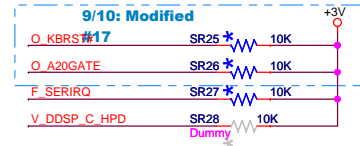
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<4> S_SATA_LED#



SR154 (unstuff)change to SR143 (stuff) 0407

Chassis ID

ID2	ID1	ID0	Type
1	0	1	SFF(Mr. Big)
1	0	0	DT(Motley Crue)
0	0	0	MT(Bon Jovi)
0	1	1	Wenger

BOARD ID

Rev1	Rev0	Type
0	0	Default
0	1	Reserved
1	0	Reserved
1	1	Reserved

PCH_CONFIG

Need to check

S_PCH_CONFIG_JUMPER

S_PCH_CONFIG_JUMPER

S_PCH_CONFIG_JUMPER

S_PCH_CONFIG_JUMPER

S_PCH_CONFIG_JUMPER

S_PCH_CONFIG_JUMPER

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S_PCH_CONFIG_JUMPER



Title

PCH-3:SATA/HOST/FAN

DWG NO

Wembley_MT

Rev

A01

Date:

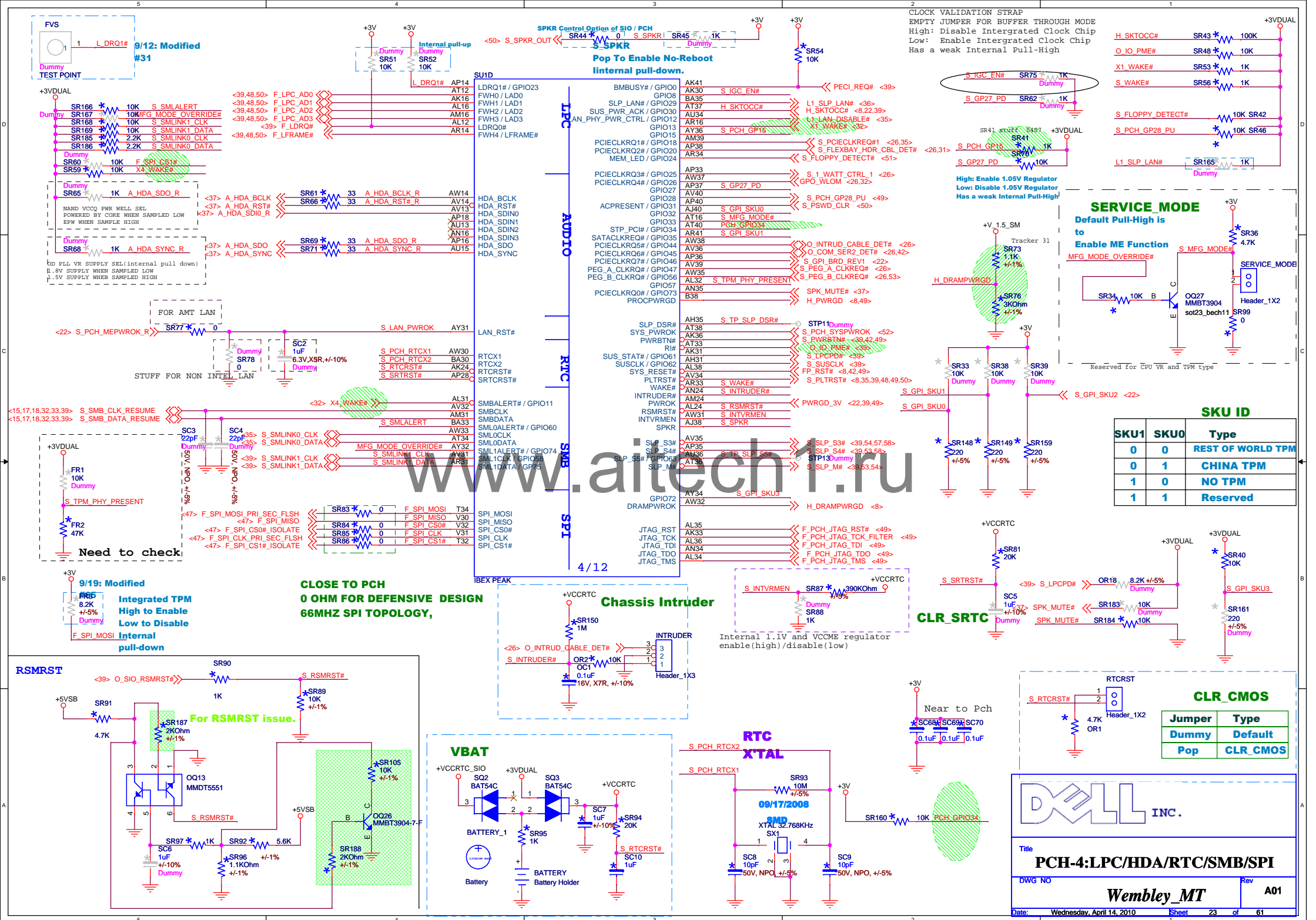
Wednesday, April 14, 2010

Sheet

22

of

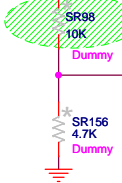
61



0424 add Depop SR98, NV_ALE

+3v change to +V_NAND_IO follow CRB1.1

+V_NAND_IO



S_NVR_CLE internal pull-down.

SR100
10K
Dummy

SU1E
NV_ALE NV_DQ0/NV_IO0
NV_CLE NV_DQ1/NV_IO1
NV_RE# NV_DQ2/NV_IO2
S_NVR_RB N NV_DQ3/NV_IO3
S_NVR_RE_RB0 N NV_DQ4/NV_IO4
S_NVR_RE_RB1 N NV_DQ5/NV_IO5
S_NVR_CK0 N NV_DQ6/NV_IO6
S_NVR_CK1 N NV_DQ7/NV_IO7
NV_WE#_CK0 NV_DQ8/NV_IO8
NV_WE#_CK1 NV_DQ9/NV_IO9
NV_DQ10/NV_IO10
NV_DQ11/NV_IO11
NV_DQ12/NV_IO12
NV_DQ13/NV_IO13
NV_DQ14/NV_IO14
NV_DQ15/NV_IO15

NVRAM

5/12

IBEX PEAK

SU1G

FDILINK

7/12

IBEX PEAK

FDI_RXN0 H_FDI_TX_DN0 <9>
FDI_RXP0 H_FDI_TX_DP0 <9>
FDI_RXN1 H_FDI_TX_DN1 <9>
FDI_RXP1 H_FDI_TX_DP1 <9>
FDI_RXN2 H_FDI_TX_DN2 <9>
FDI_RXP2 H_FDI_TX_DP2 <9>
FDI_RXN3 H_FDI_TX_DN3 <9>
FDI_RXP3 H_FDI_TX_DP3 <9>
FDI_RXN4 H_FDI_TX_DN4 <9>
FDI_RXP4 H_FDI_TX_DP4 <9>
FDI_RXN5 H_FDI_TX_DN5 <9>
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FDI_RXP7 H_FDI_TX_DP7 <9>
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FDI_LSYNC1 H_FDI_LSYNC1 <9>
FDI_INT H_FDI_INT <9>

9/12: DG 0.8 Modified
#37

L36 SR104 32.4
+/-1%

T33 S_NVR_DATA0
P35 S_NVR_DATA1
T31 S_NVR_DATA2
P33 S_NVR_DATA3
M35 S_NVR_DATA4
L33 S_NVR_DATA5
M36 S_NVR_DATA6
M34 S_NVR_DATA7
M30 S_NVR_DATA8
F36 S_NVR_DATA9
F37 S_NVR_DATA10
E39 S_NVR_DATA11
G33 S_NVR_DATA12
D40 S_NVR_DATA13
F33 S_NVR_DATA14
F33 S_NVR_DATA15
H36 S_NVR_CE_N0
H35 S_NVR_CE_N1
P32 S_NVR_CE_N2
E41 S_NVR_CE_N3
P36 S_NVR_RDSTRBIO
F40 S_NVR_RDSTRBI1

S_NVR_CE_N0
S_NVR_CE_N1
S_NVR_CE_N2
S_NVR_CE_N3

S_NVR_RE_RB0 N
S_NVR_RE_RB1 N
S_NVR_RB N
S_NVR_ALE
S_NVR_CLE

S_NVR_CK0 N
S_NVR_CK1 N

+V_NAND_IO

DEFENSIVE DESIGN
PULL UP ON NVRAM MODULE

S_NVR_DATA0
S_NVR_DATA1
S_NVR_DATA2
S_NVR_DATA3
S_NVR_RDSTRBIO
S_NVR_DATA4
S_NVR_DATA5
S_NVR_DATA6
S_NVR_DATA7
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S_NVR_DATA10
S_NVR_DATA11
S_NVR_DATA12
S_NVR_DATA13
S_NVR_DATA14
S_NVR_DATA15
S_NVR_RDSTRBI1

S_NVR_CE_N0
S_NVR_CE_N1
S_NVR_CE_N2
S_NVR_CE_N3

S_NVR_RE_RB0 N
S_NVR_RE_RB1 N
S_NVR_RB N
S_NVR_ALE
S_NVR_CLE

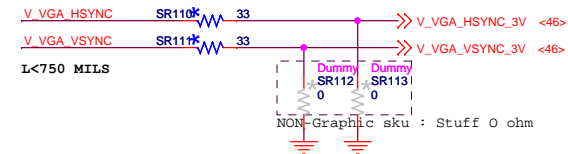
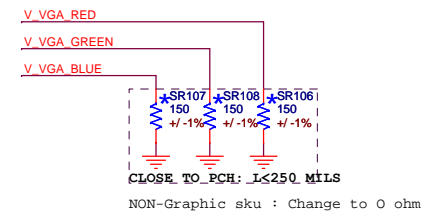
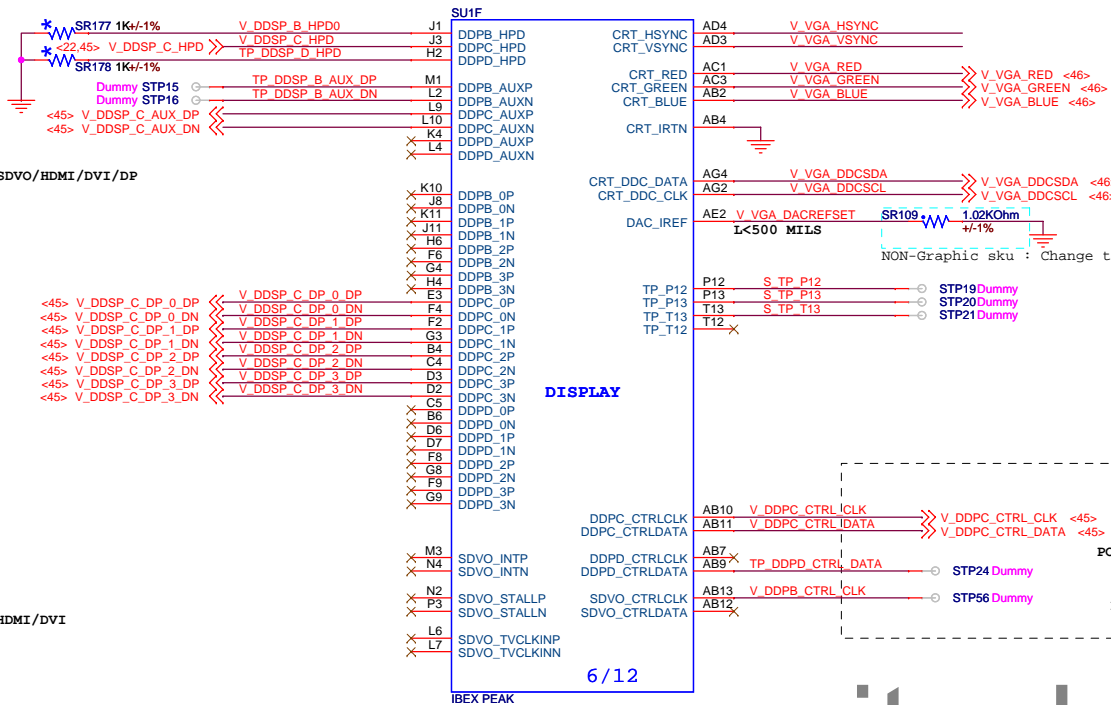
S_NVR_CK0 N
S_NVR_CK1 N

+V_NAND_IO

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DQ1393
DQ1394
DQ13

HPD needs be grounded on unused(ground via 1k resistor).
Follow Design Guide 1.0



07/12
BEX PEAK
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Title

PCH-7:DISPLAY

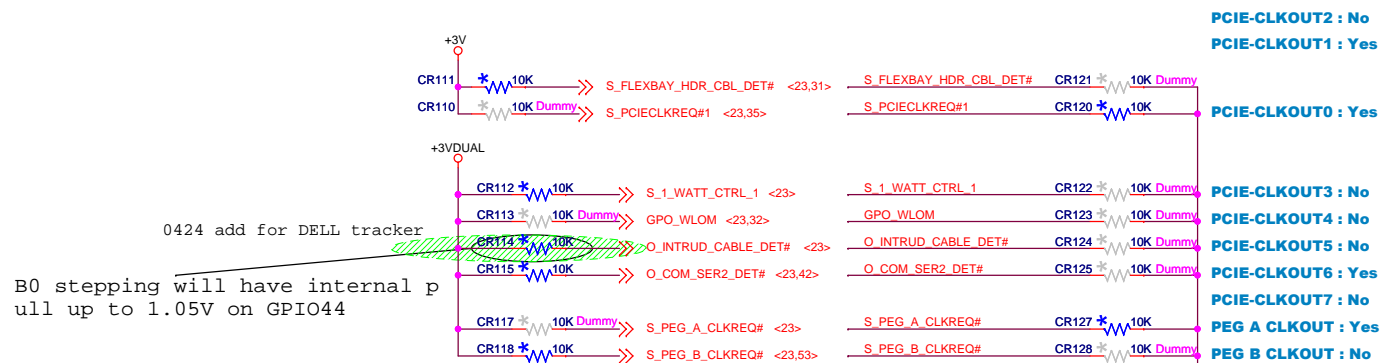
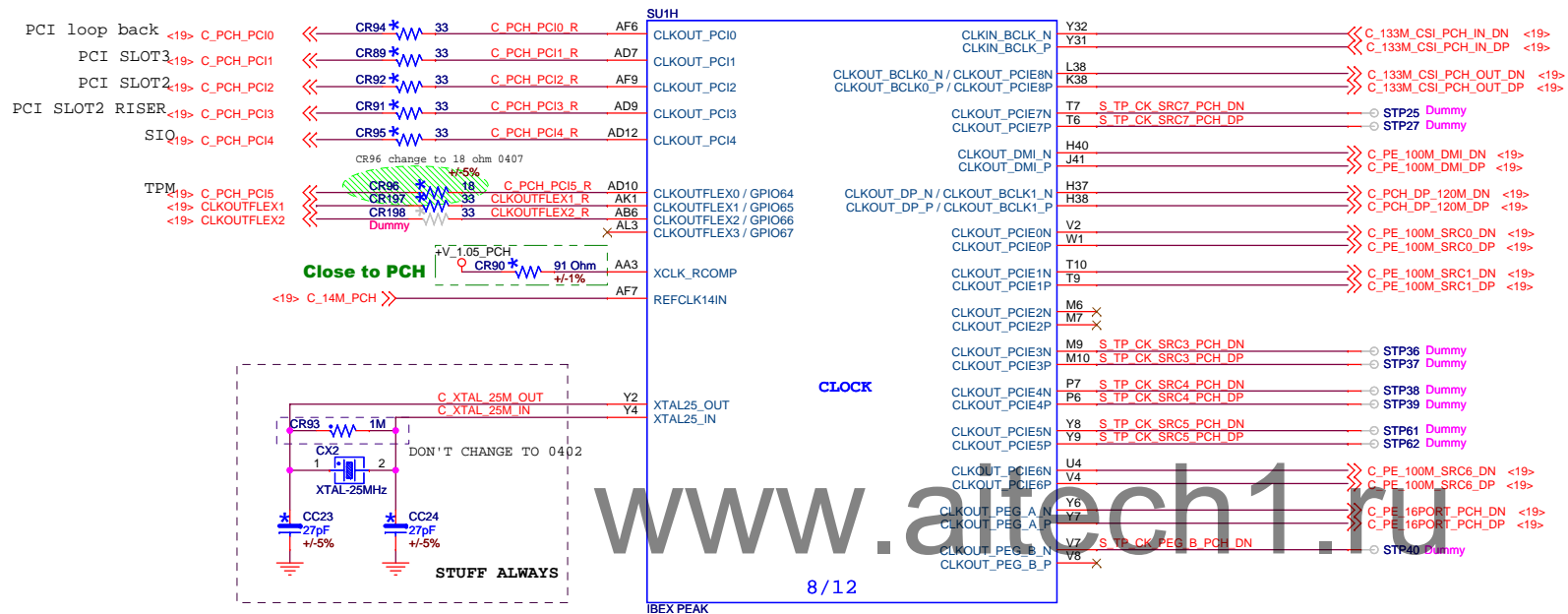
DWG NO	
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Wembley MT

Rev	A01
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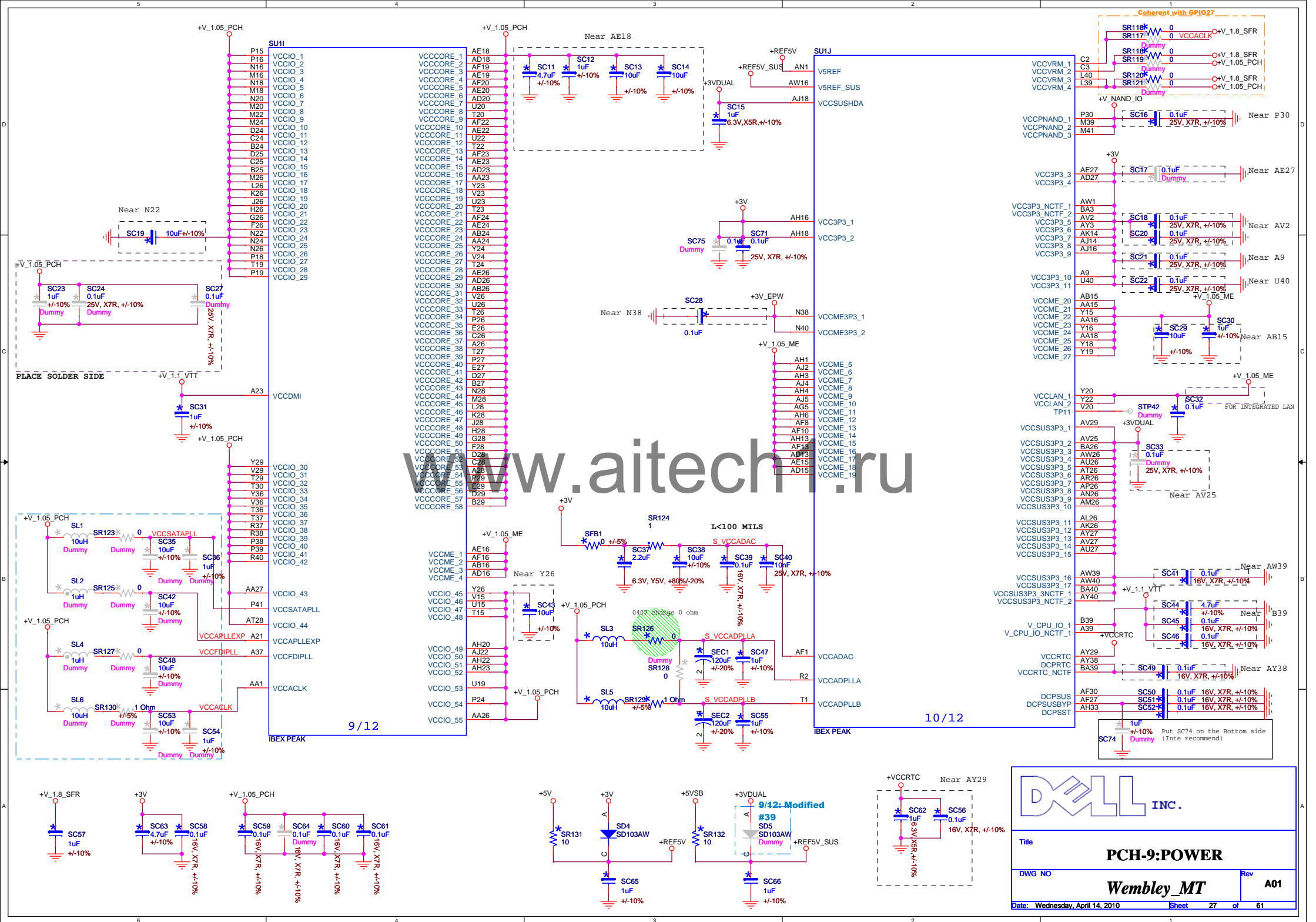
Date: Wednesday, April 14, 2010

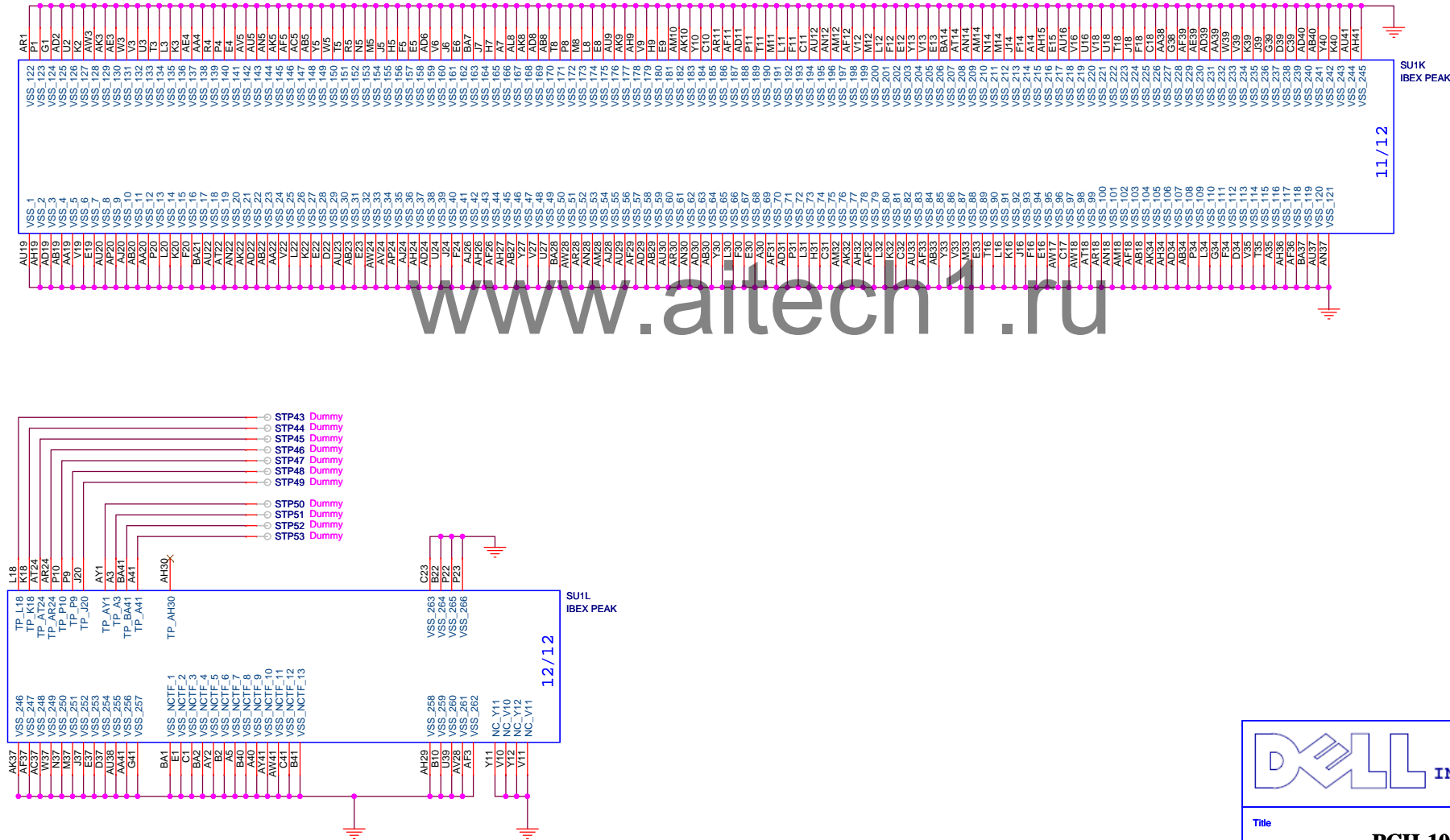
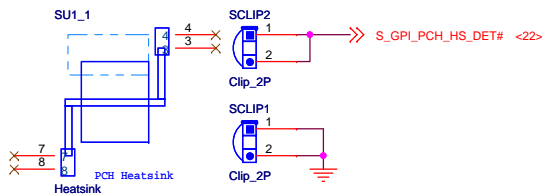
Sheet 25 of 61



9/11: CRB 1.0
 Modified #20

Title		
PCH-8:CLOCK		
DWG NO	Rev	A01
Wembley_MT		
Date: Wednesday, April 14, 2010	Sheet 26	of 61





Title

PCH-10:GND

DWG NO

Wembley_MT

Date: Wednesday, April 14, 2010

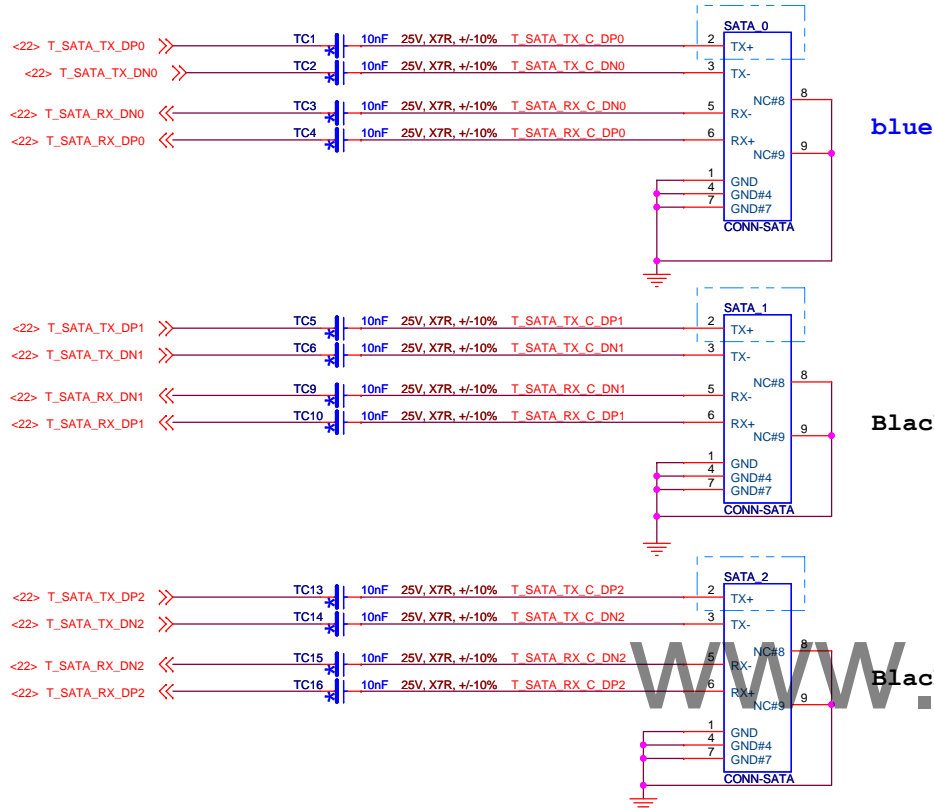
Rev

A01

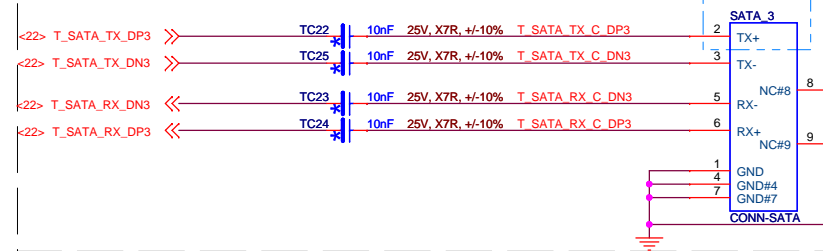
Sheet 28 of 61

SATA x 3

Need to Sub Connector Color

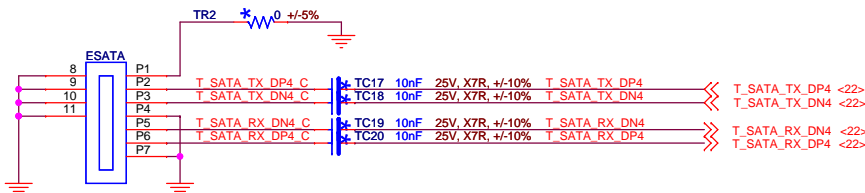


SATA port 3 only for MT Black



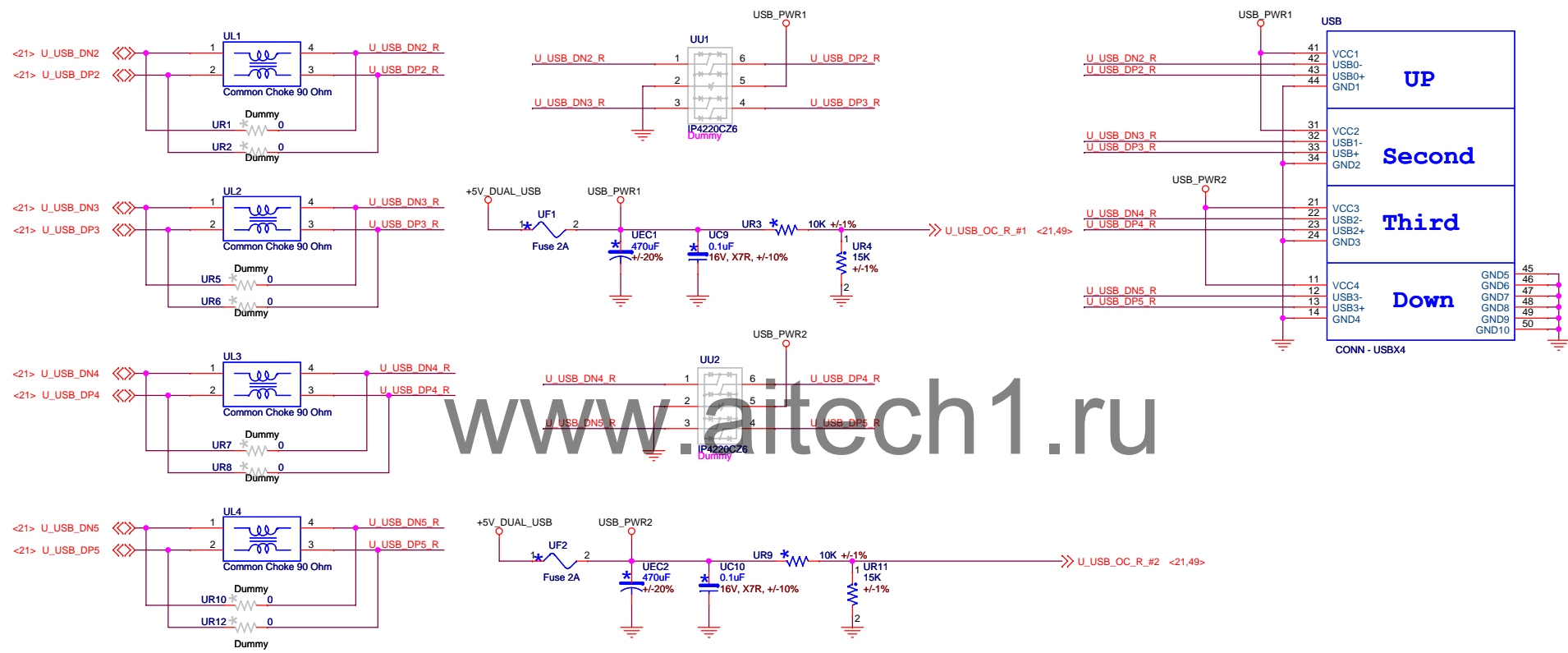
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E SATA



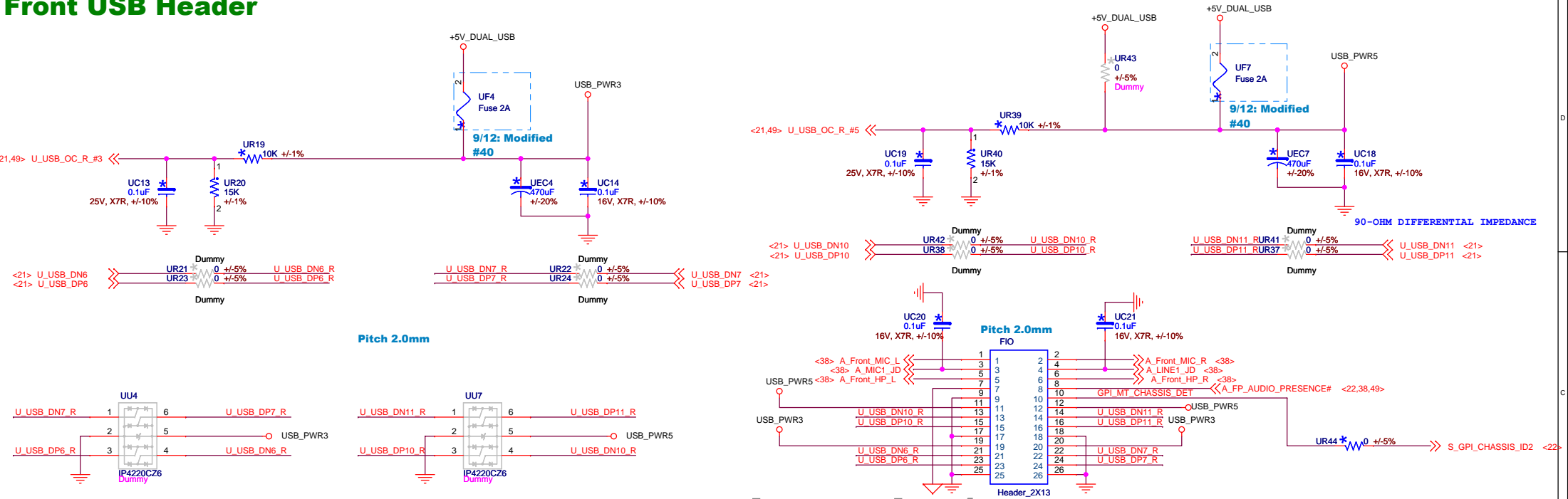
DELL INC.	
Title	
SATAx3 / eSATA	
DWG NO	Rev
Wembley_MT	A01
Date: Wednesday, April 14, 2010	Sheet 29 of 61

Rear USB CONNECTOR

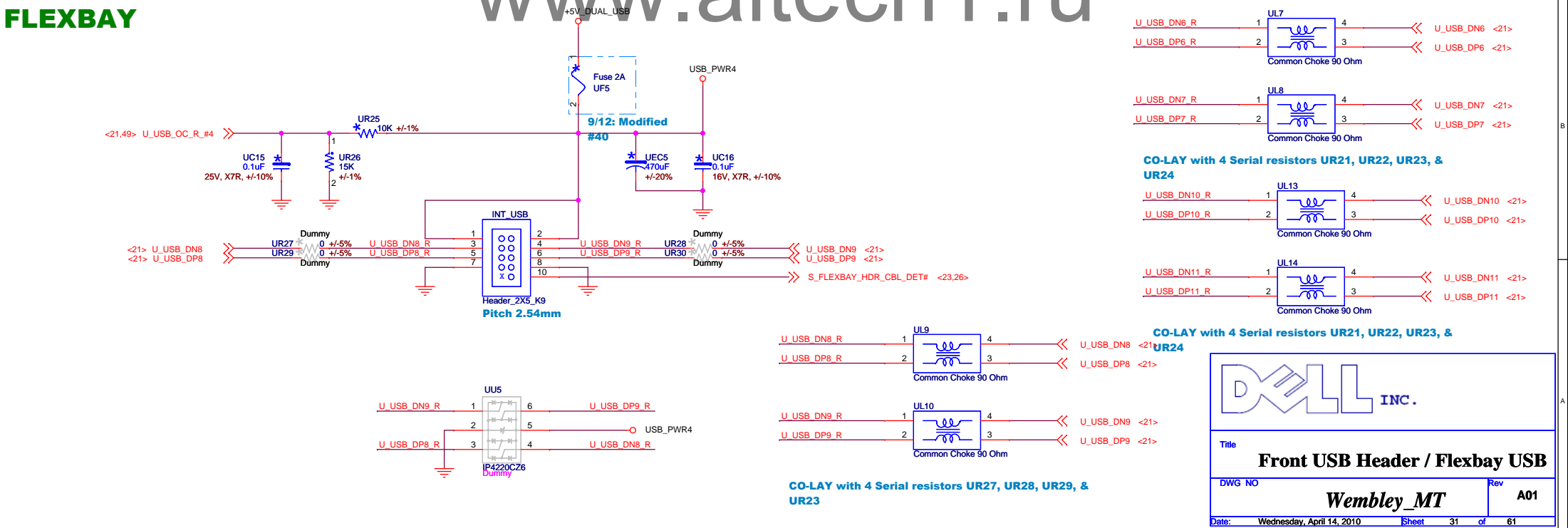


Title		Rear USB	
DWG NO		Wembley_MT	
Date: Wednesday, April 14, 2010		Sheet 30 of 61	

Front USB Header



FLEXBAY



Title

Front USB Header / Flexbay USB

DWG NO

Wembley_MT

Date: Wednesday, April 14, 2010

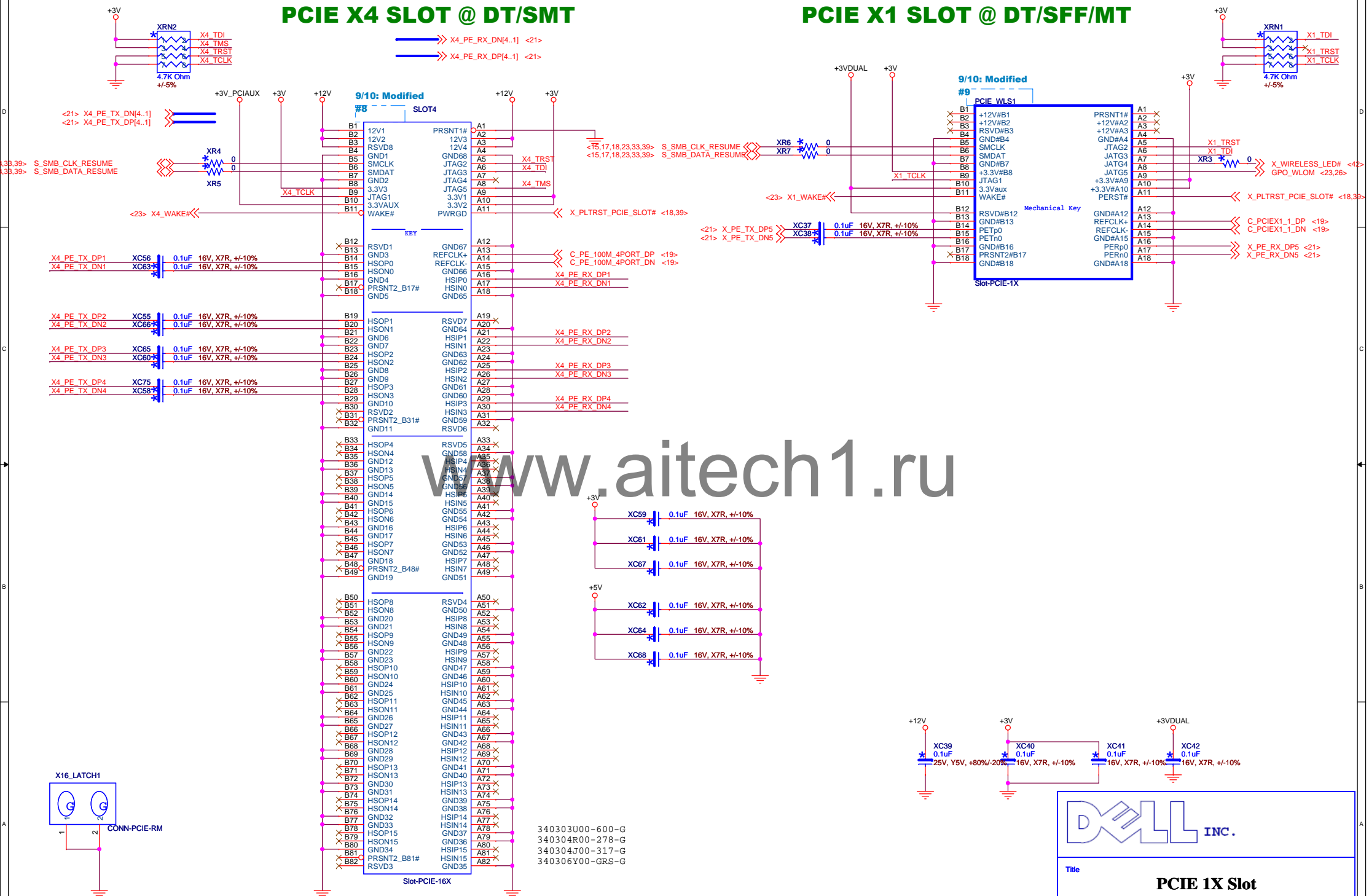
Sheet 31 of 61

Rev

A01

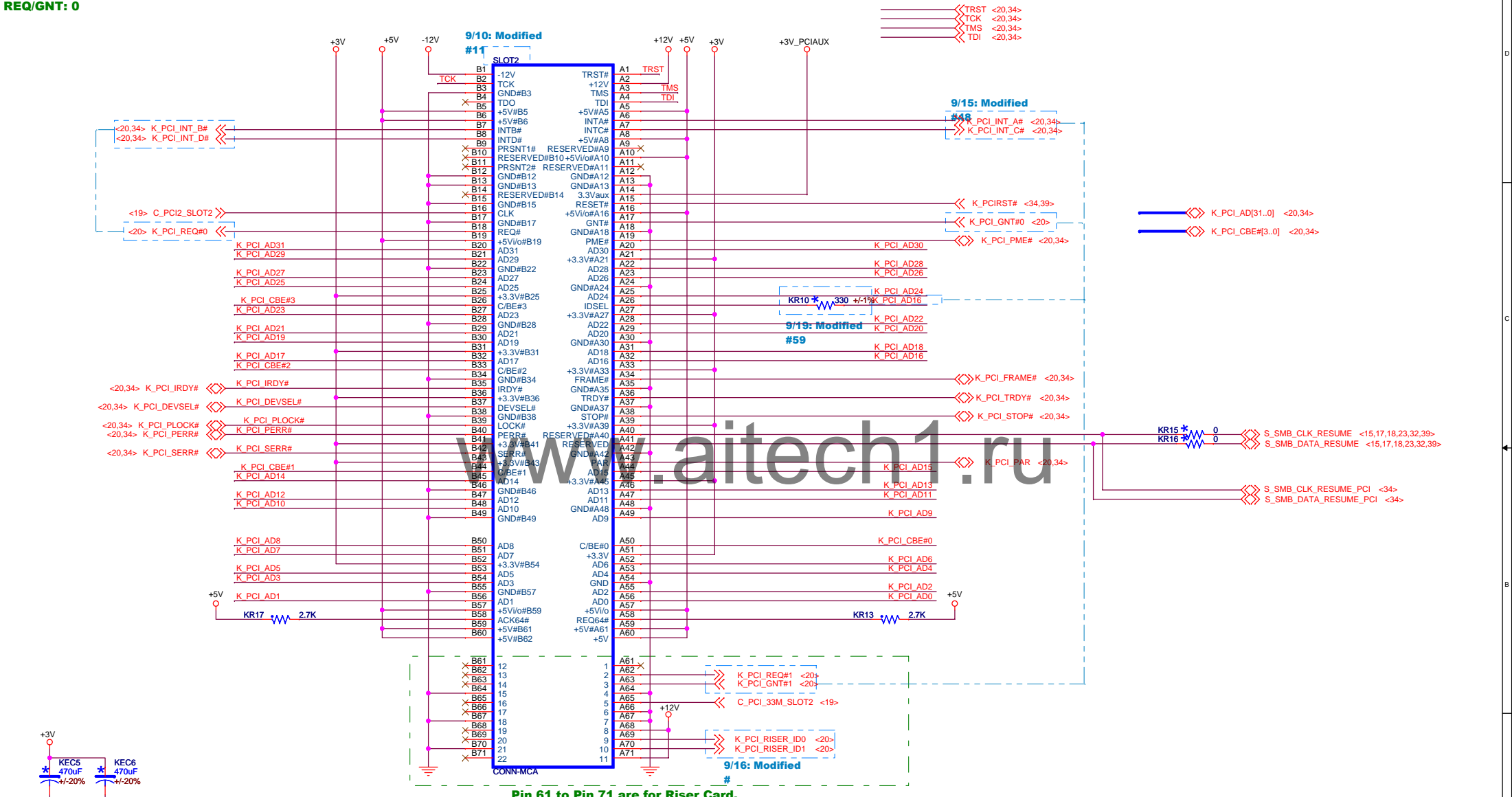
PCIE X4 SLOT @ DT/SMT

PCIE X1 SLOT @ DT/SFF/MT



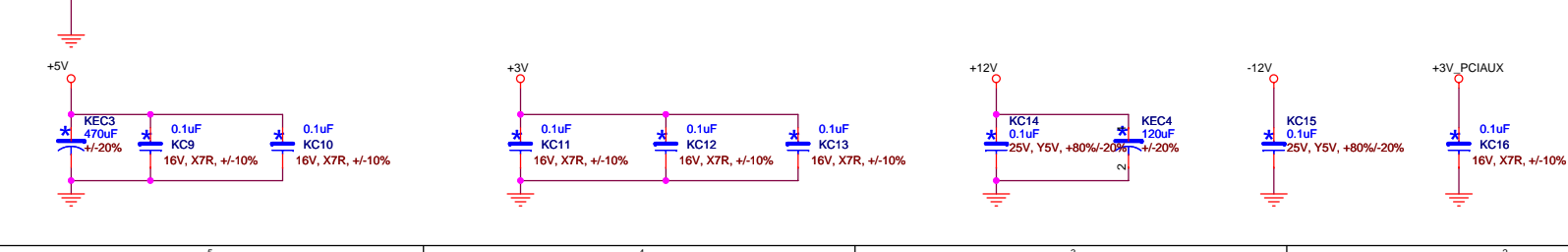
PCI SLOT 2 with Riser Card @ DT


IRQ: ABCD For Riser
IDSEL: AD16 REQ/GNT: 1
REQ/GNT: 0



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Pin 61 to Pin 71 are for Riser Card.



**INC.**

Title

PCI SLOT 2

DWG NO

Wembley_MT

Date

Wednesday, April 14, 2010

Sheet

33

Rev

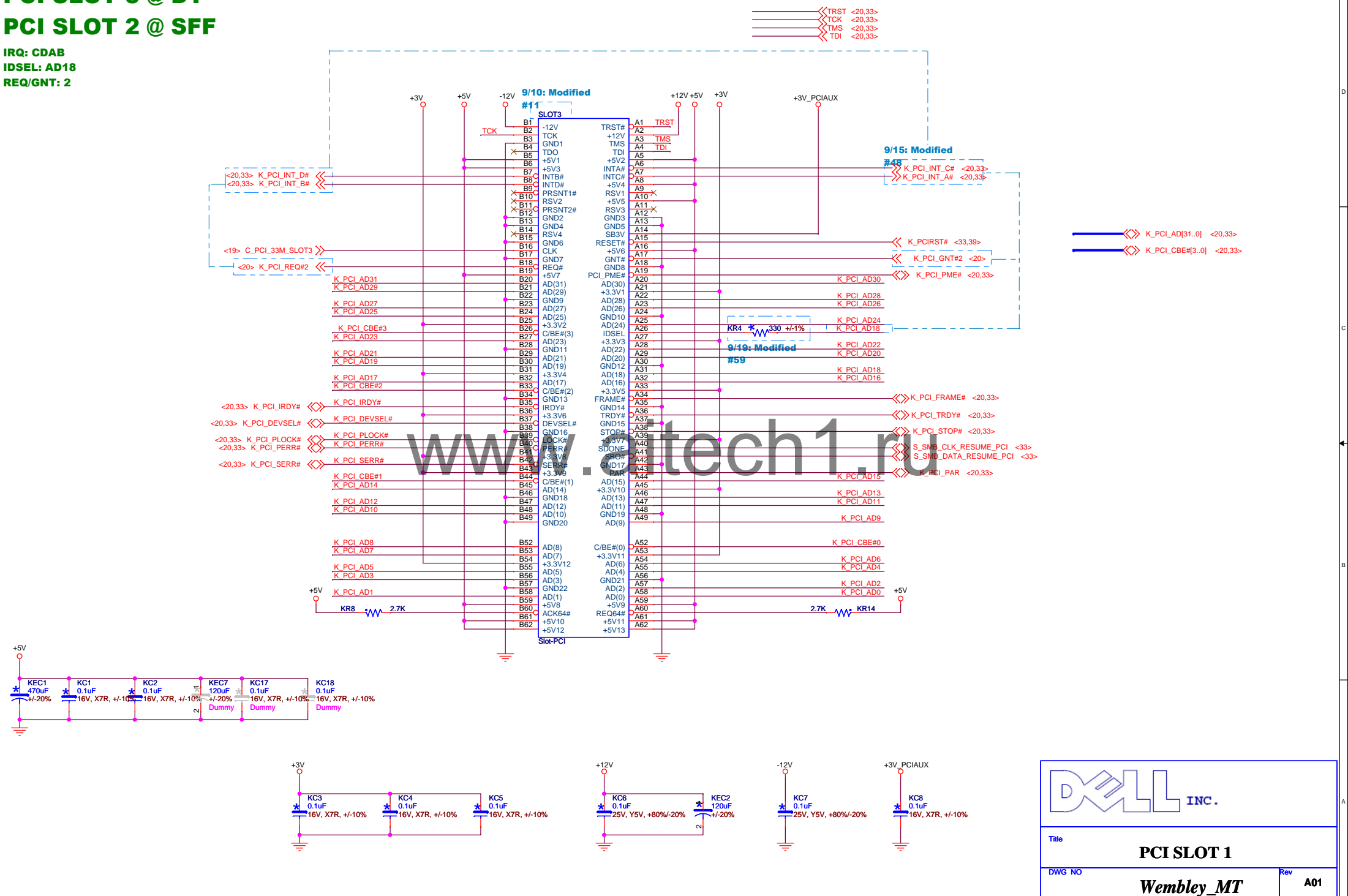
A01


of

61

PCI SLOT 3 @ DT
PCI SLOT 2 @ SFF

IRQ: CDAB
IDSEL: AD18
REQ/GNT: 2





INC.

Title

PCI SLOT 1

DWG NO

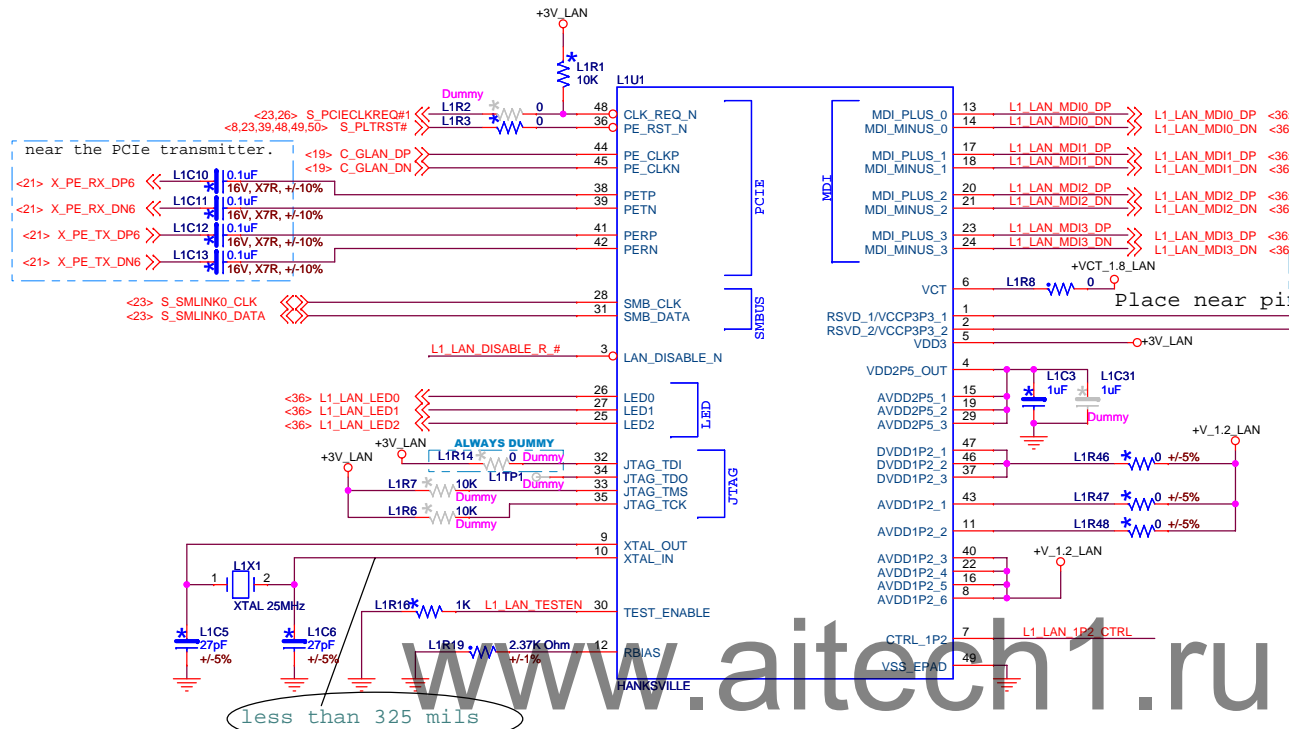
Wembley_MT

Date: Wednesday, April 14, 2010

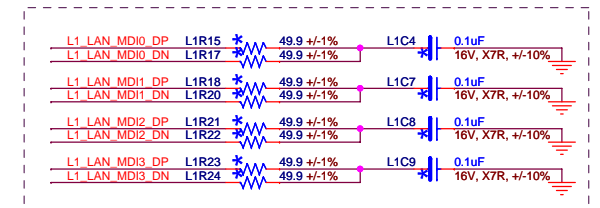
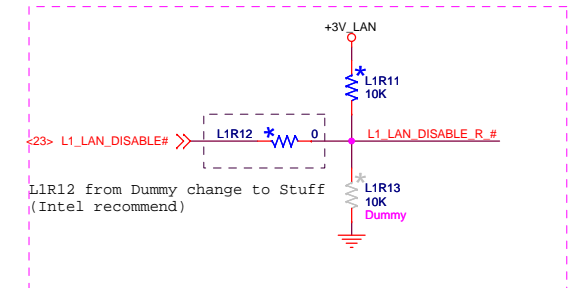
Sheet 34 of 61

Rev

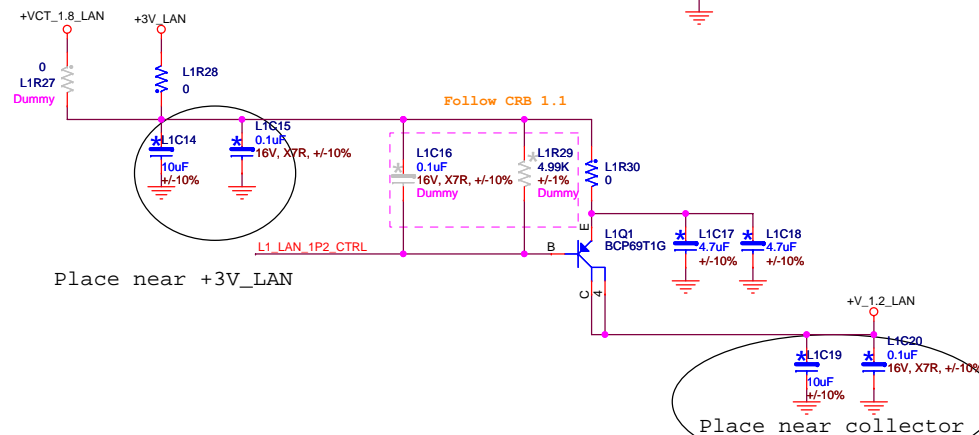
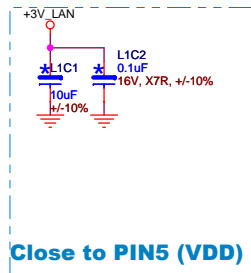
A01



9/16: 82578 GbE PHY Datasheet 0.9:
Modified #54
Need Double
Check
Different with 9.3

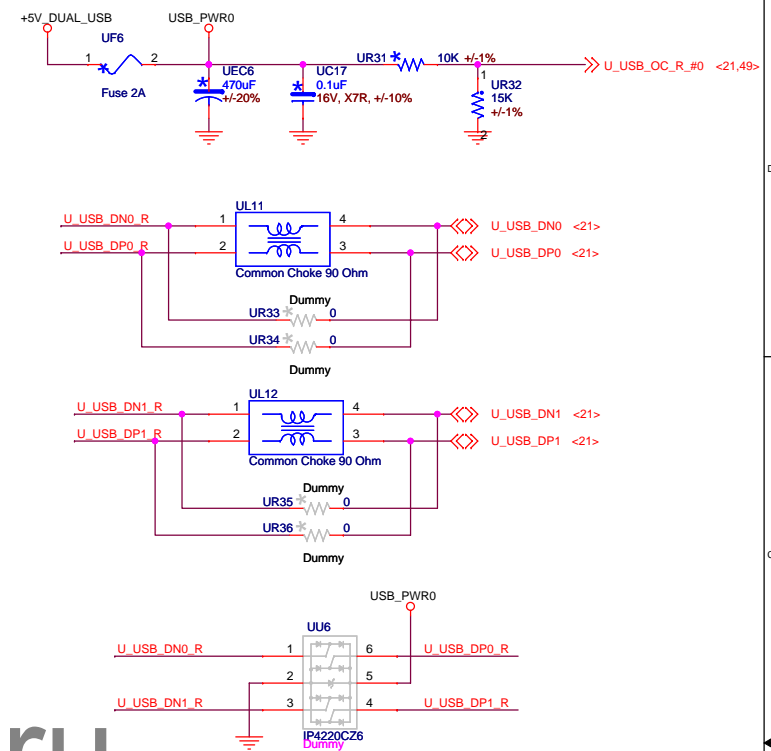
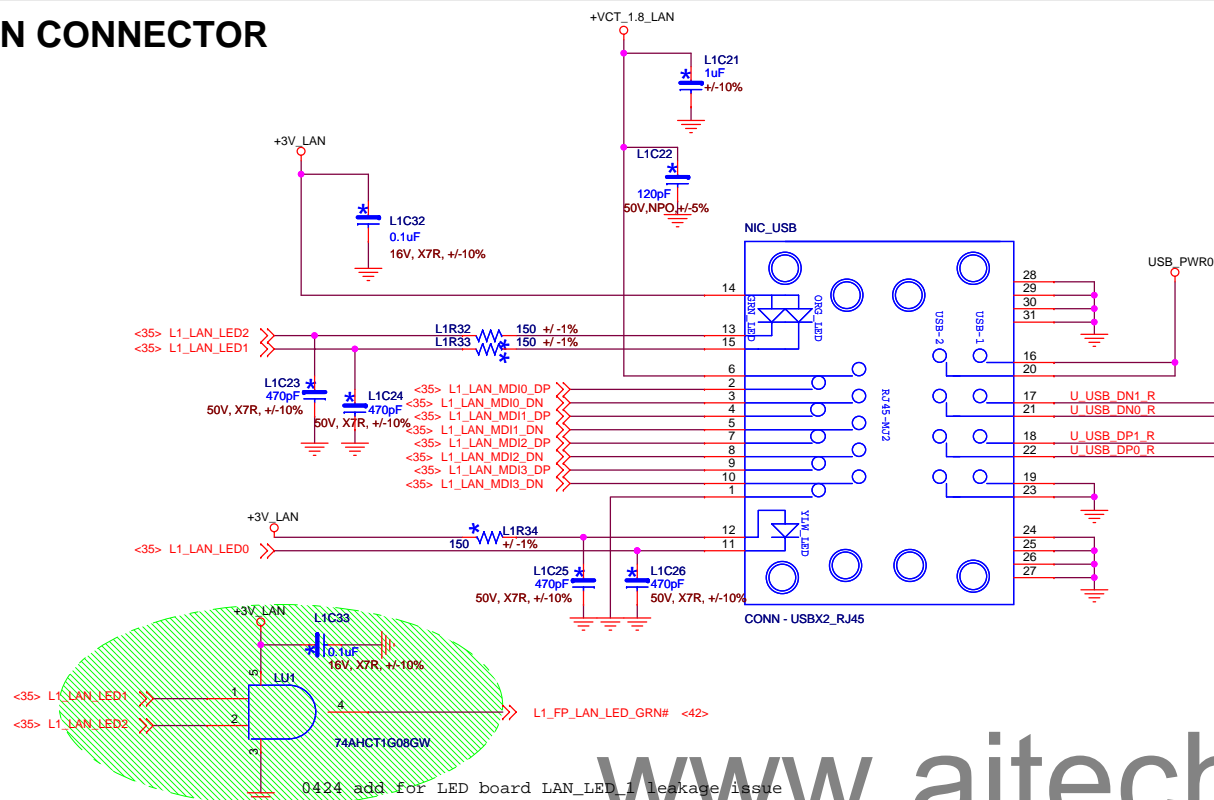


CLOSE TO PHY



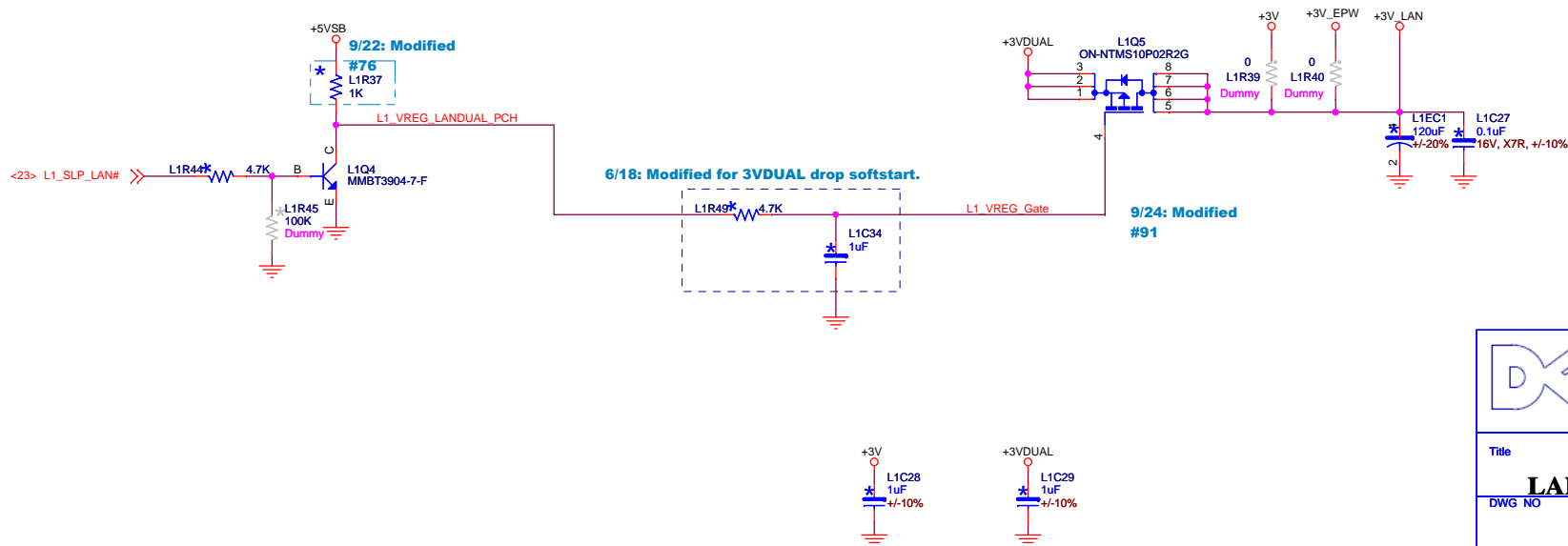
DELL INC.	
Title	
LAN:INTEL HANKSVILLE	
DWG NO	Rev
Wembley_MT	A01
Date: Wednesday, April 14, 2010	Sheet 35 of 61

LAN CONNECTOR

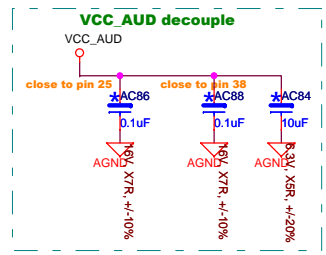
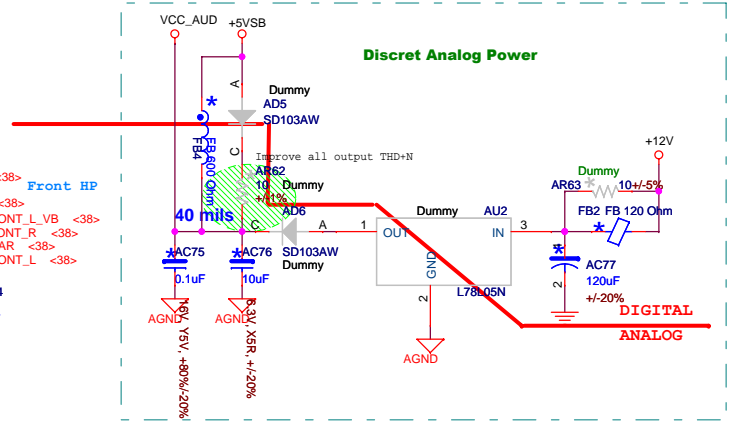
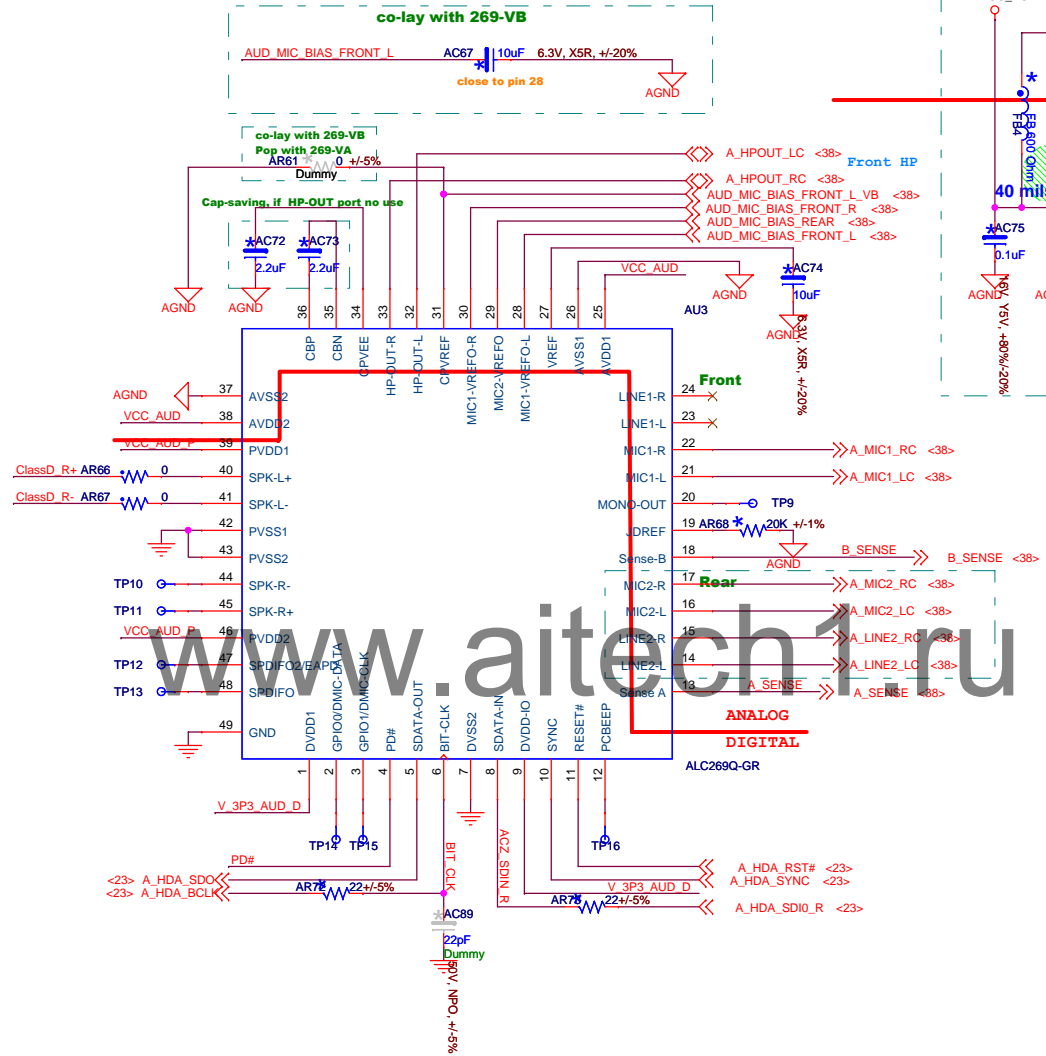
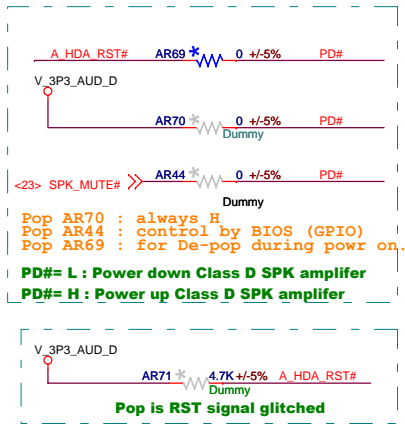
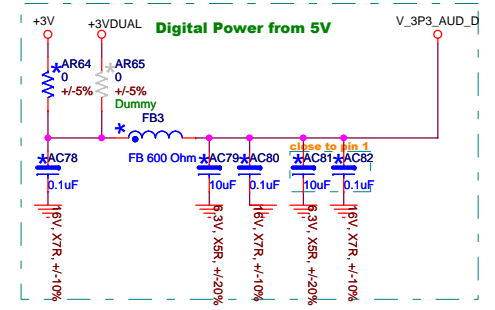
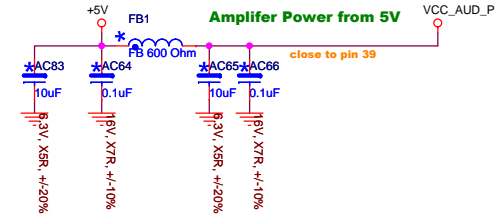


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LAN POWER



		Title	
		LAN POWER & LAN/USB CONN	
DWG NO		Rev	
Wembley_MT		A01	
Date: Wednesday, April 14, 2010		Sheet 36 of 61	

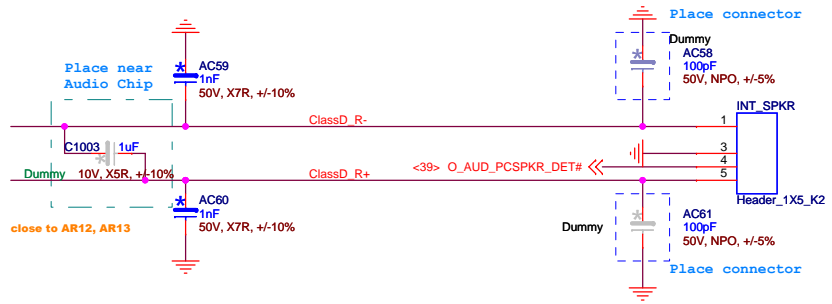


For ALC269-VB option

Dummy AD5, AD6, AR61, AR62, AU2

Stuff AC67, FB4 (0ohm)

Dummy R55, Stuff R54



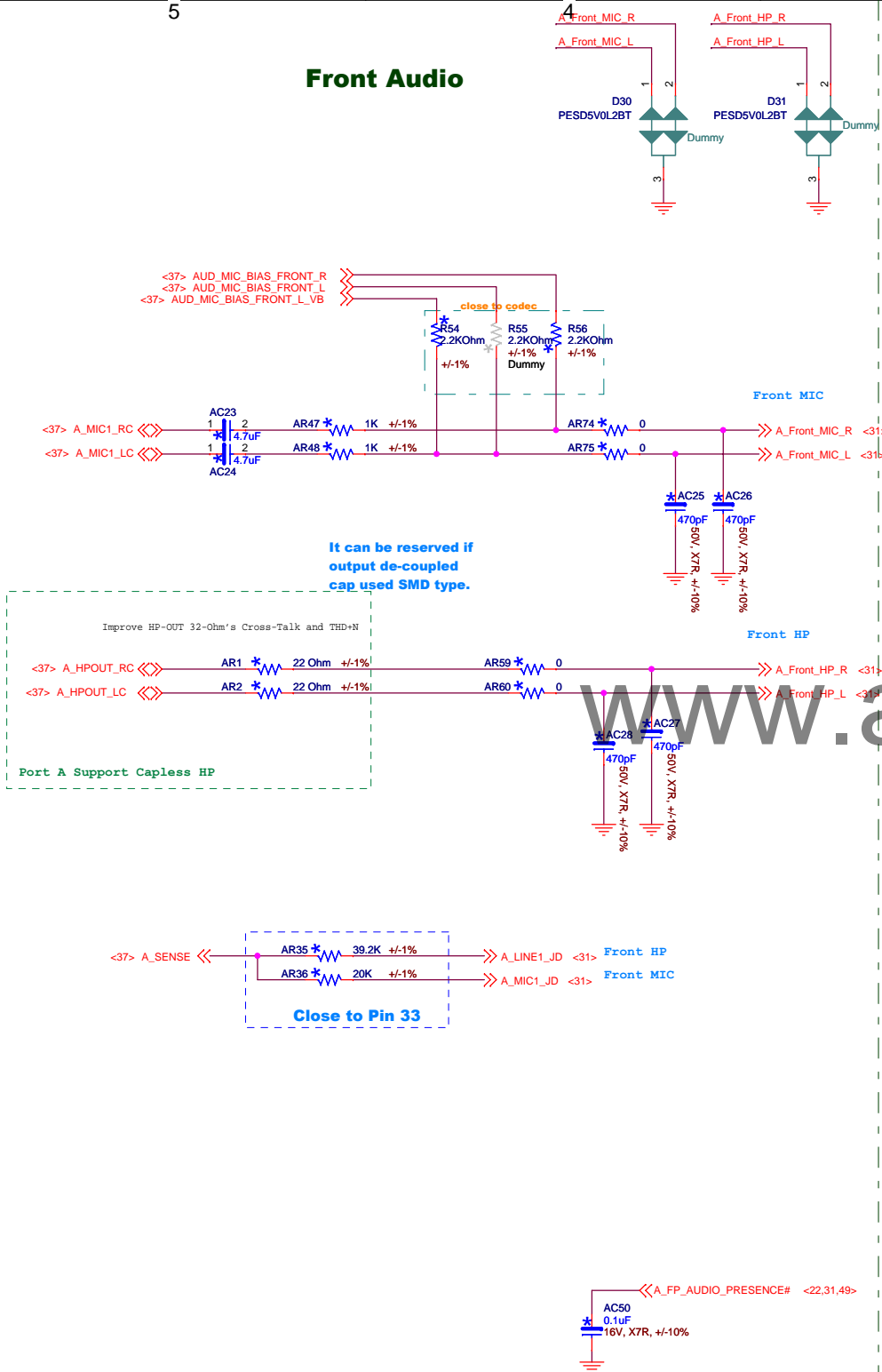
CHASSIS SPEAKER

Header 1x5 cut2

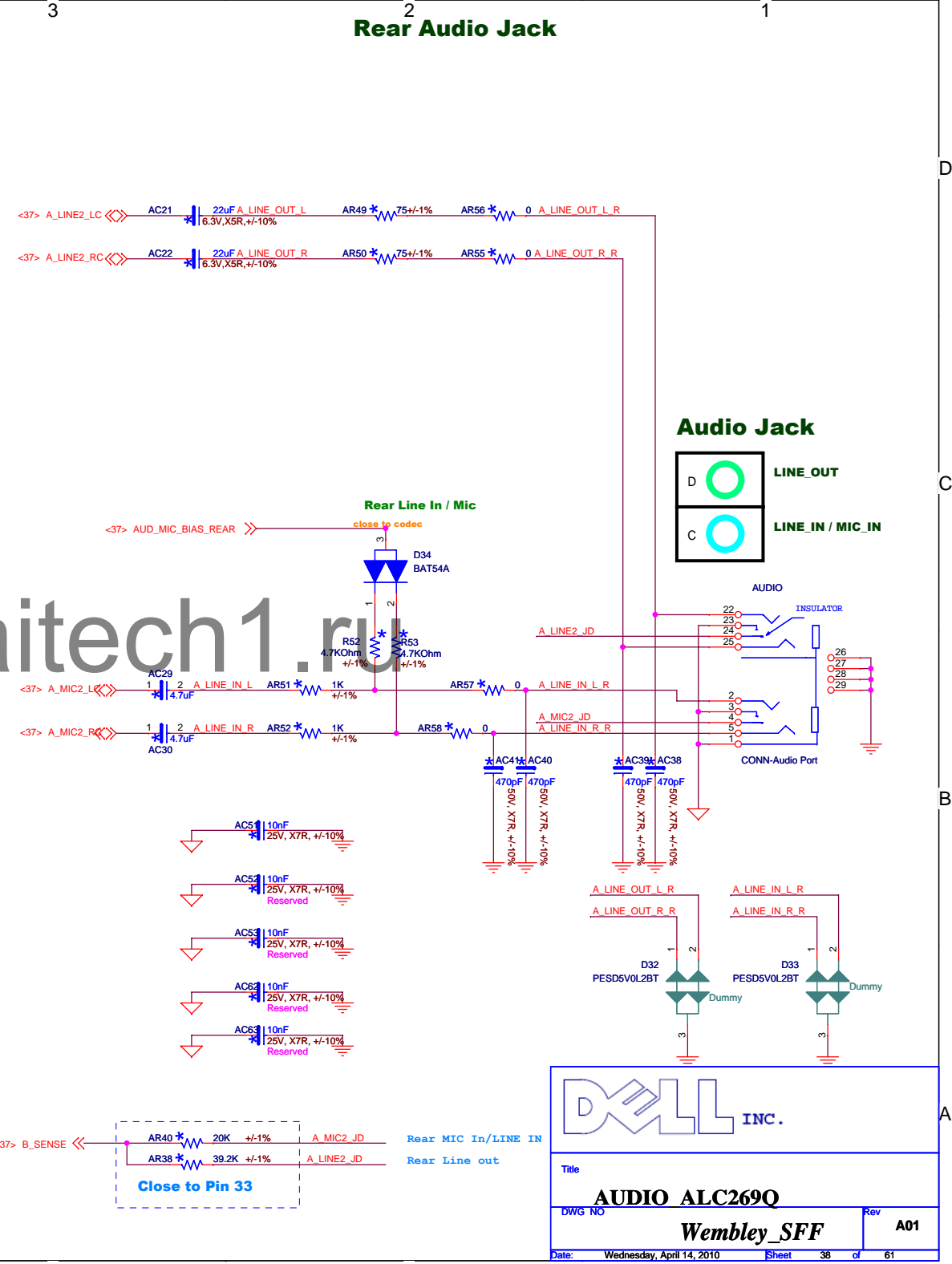
Pin.1--> Left-
 Pin.2--> NC key
 Pin.3--> GND
 Pin.4--> SPK det#
 Pin.5--> Left+

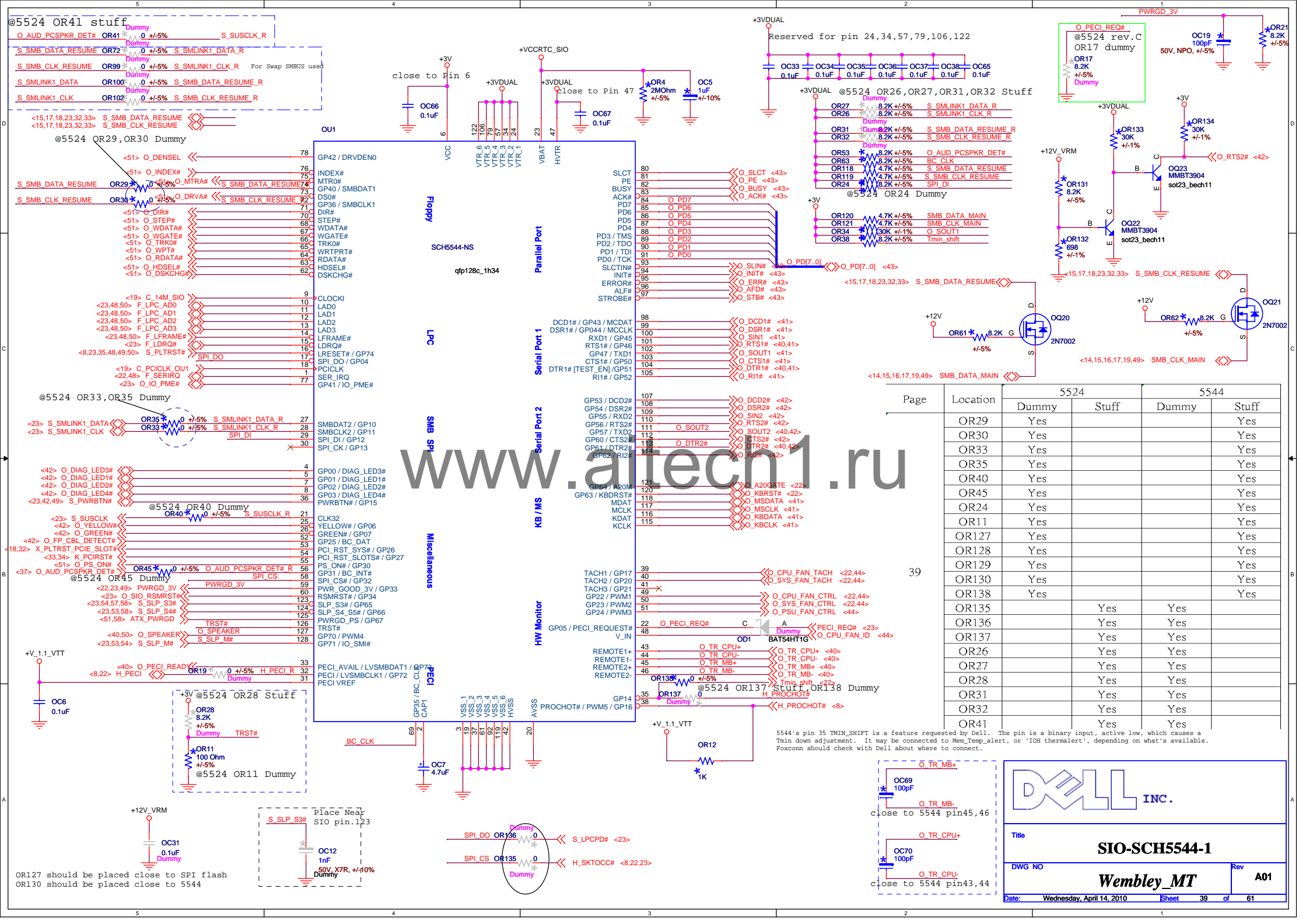
DELL INC.	
Title	
AUDIO ALC269Q	
DWG NO	Rev
Wembley_SFF	A01
Date: Wednesday, April 14, 2010	Sheet 37 of 61

Front Audio

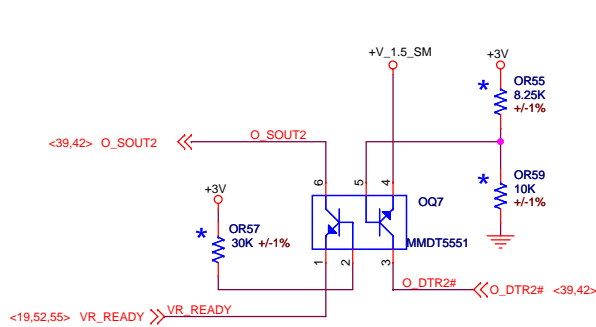
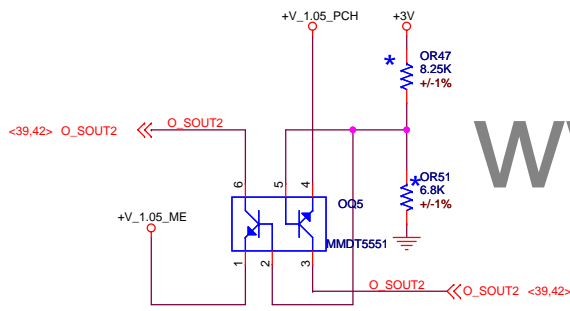
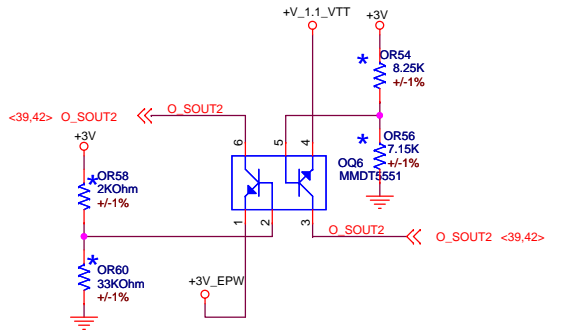
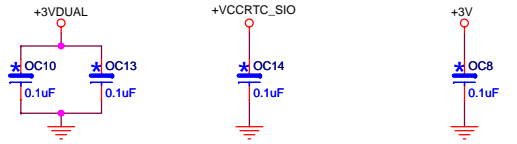


Rear Audio Jack





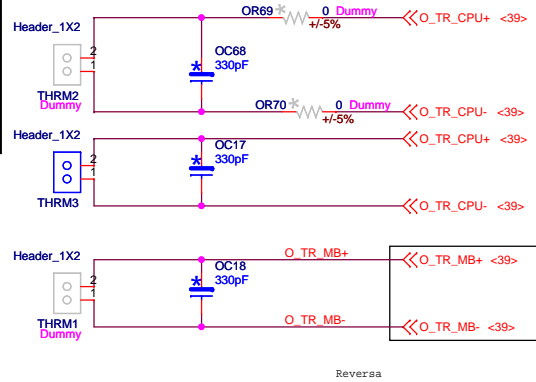
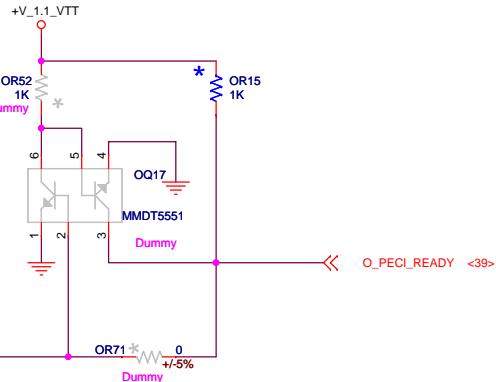
SCH5524 Decoupling



5524 PRE-POST DIAG PG GENERATION
@5514
dummy all in this block
Only used For 5524

	SPEAKER	RTS1#	DTR1#
	Diag_En	Sysopt strap	Flash_en
PULL HIGH	Disable	0 X 4E	Flash Enable
	DEFAULT	DEFAULT	DEFAULT
PULL LOW	Enable	0 X 2E	Parallel Enable

SIO STRAPING



THERMAL SENSOR

DELL INC.

Title

SIO-SCH5544-2 (Misc)

DWG NO

Wembley_MT

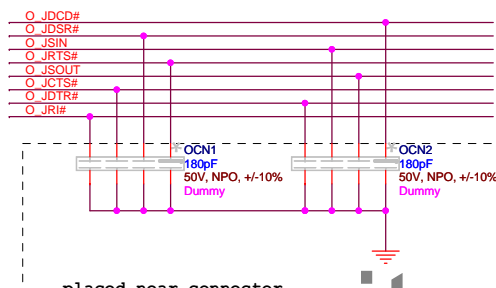
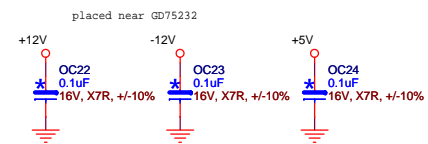
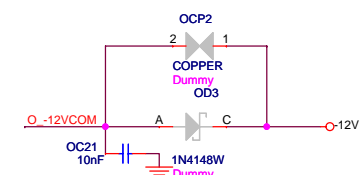
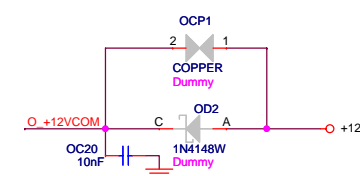
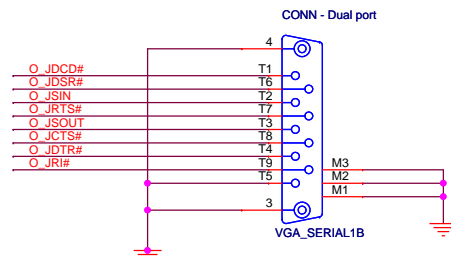
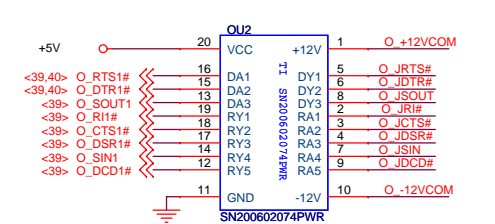
Rev

A01

Date: Wednesday, April 14, 2010

Sheet 40 of 61

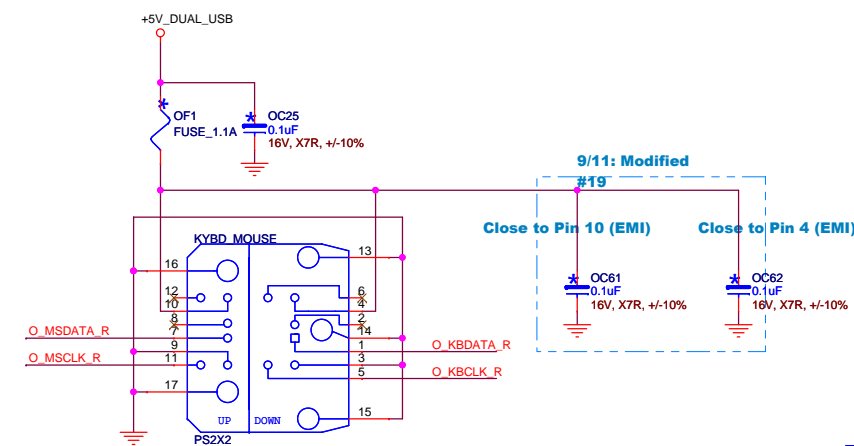
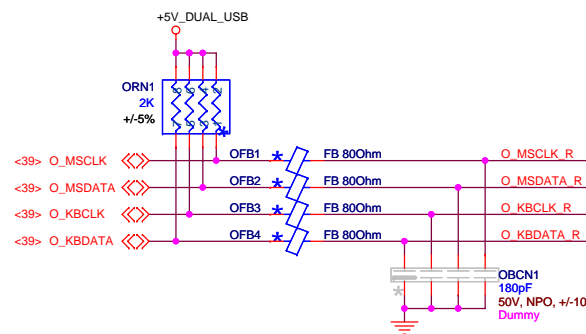
COM Port



placed near connector

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KB/MS



Title

COM Port / PS2

DWG NO

Wembley_MT

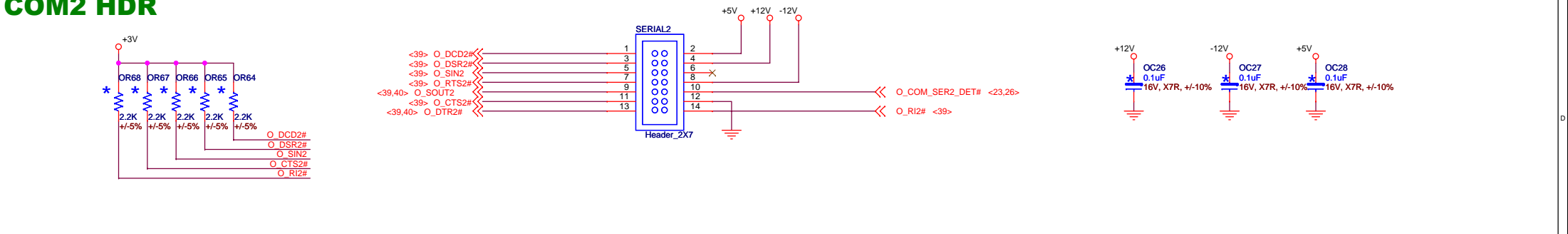
Date: Wednesday, April 14, 2010

Rev

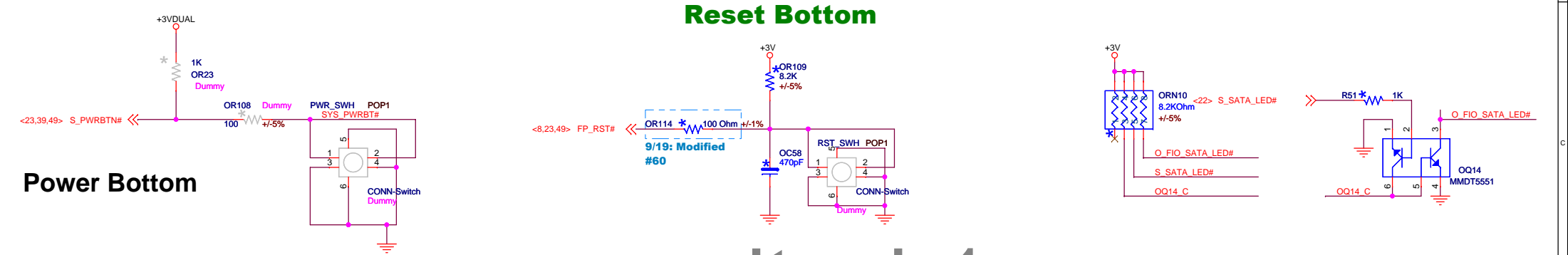
A01

Sheet 41 of 61

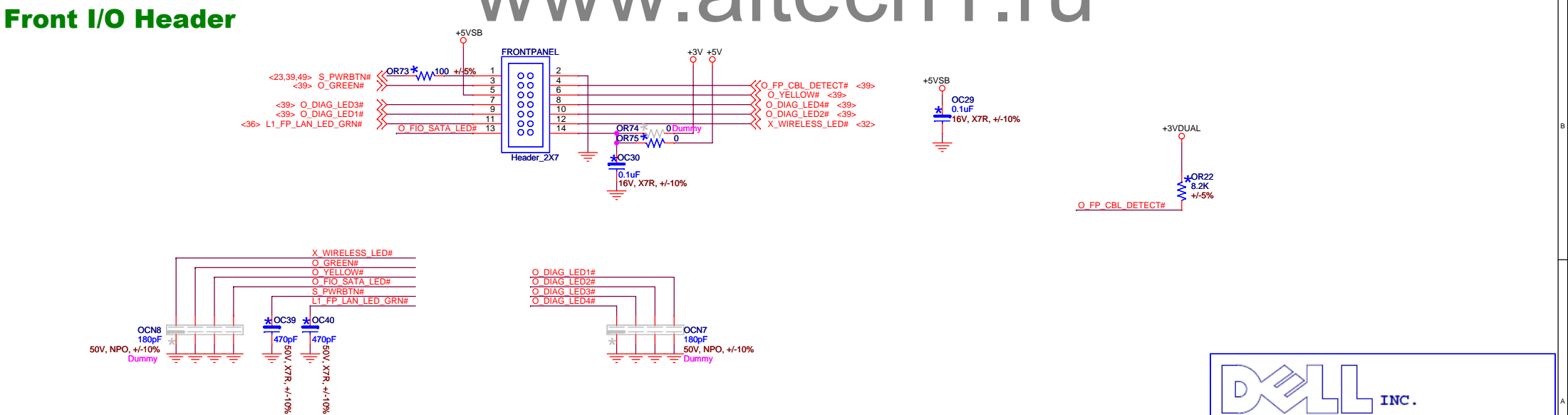
COM2 HDR



Reset Bottom



Front I/O Header



DELL INC.

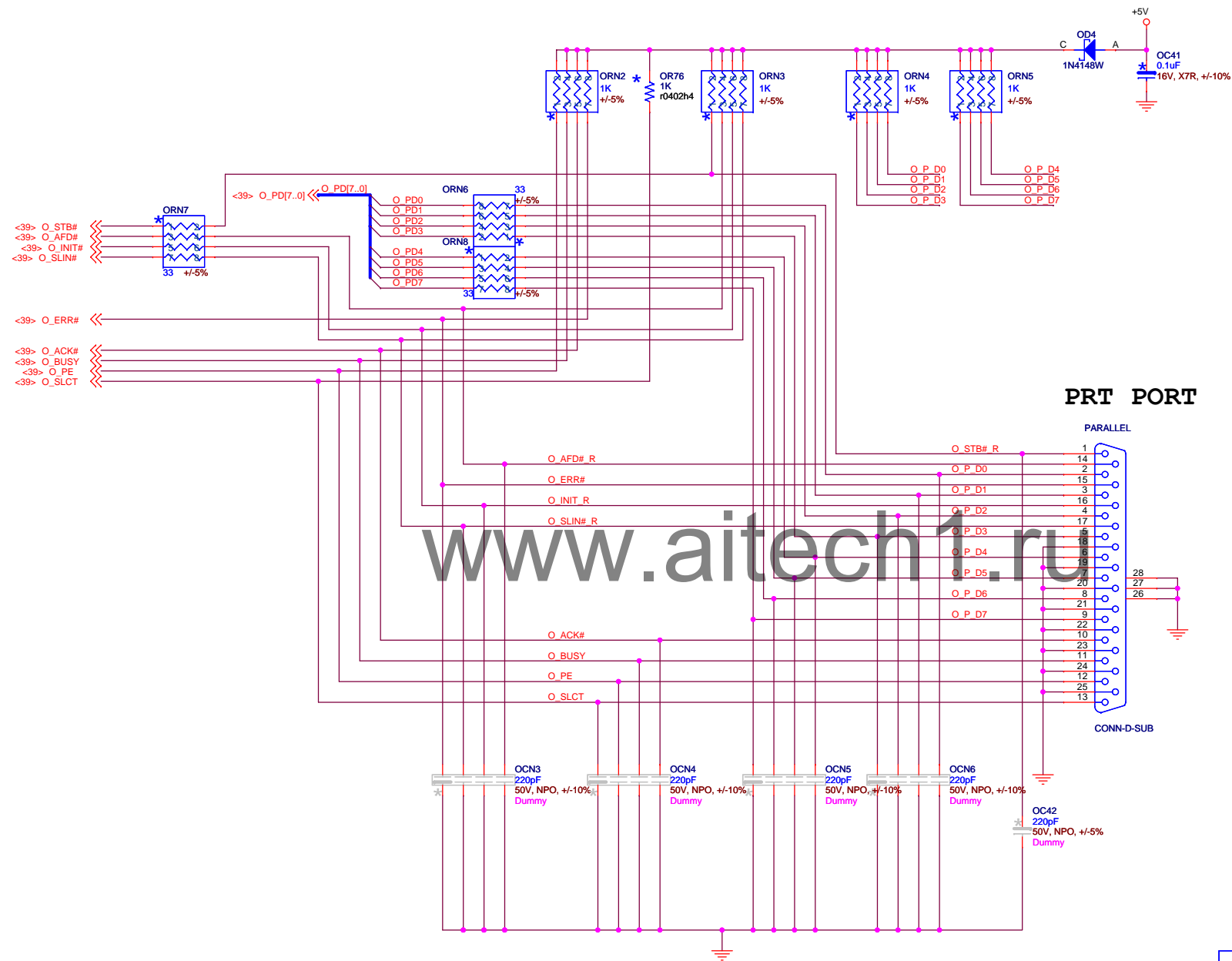
Title: Front I/O Header & COM2 HDR

DWG NO: Wembley_MT

Date: Wednesday, April 14, 2010

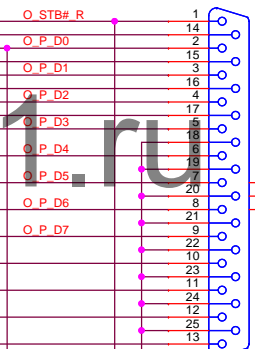
Sheet: 42 of 61

Rev: A01



PRT PORT

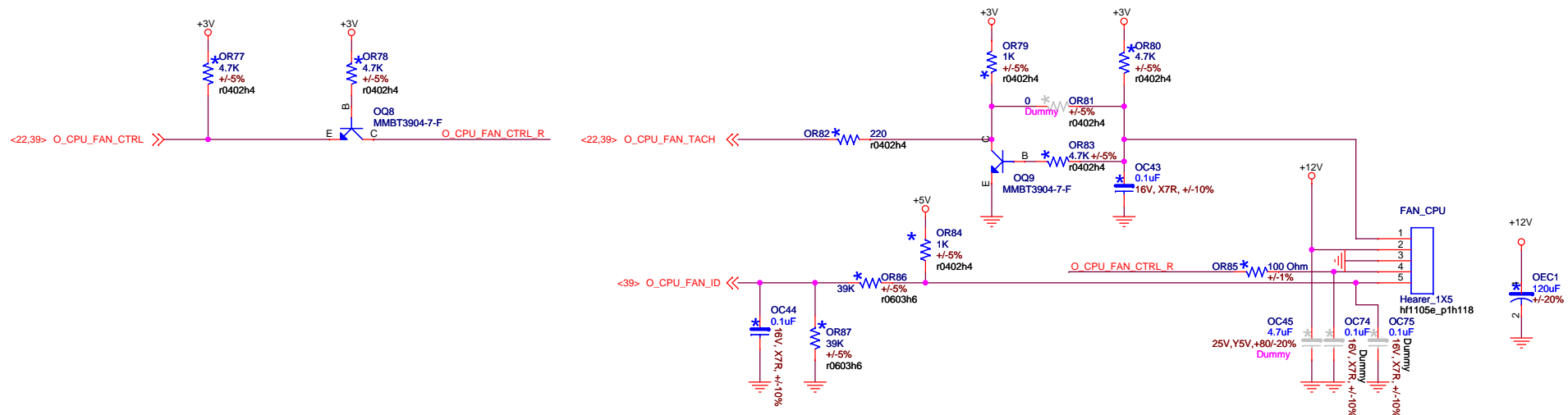
PARALLEL



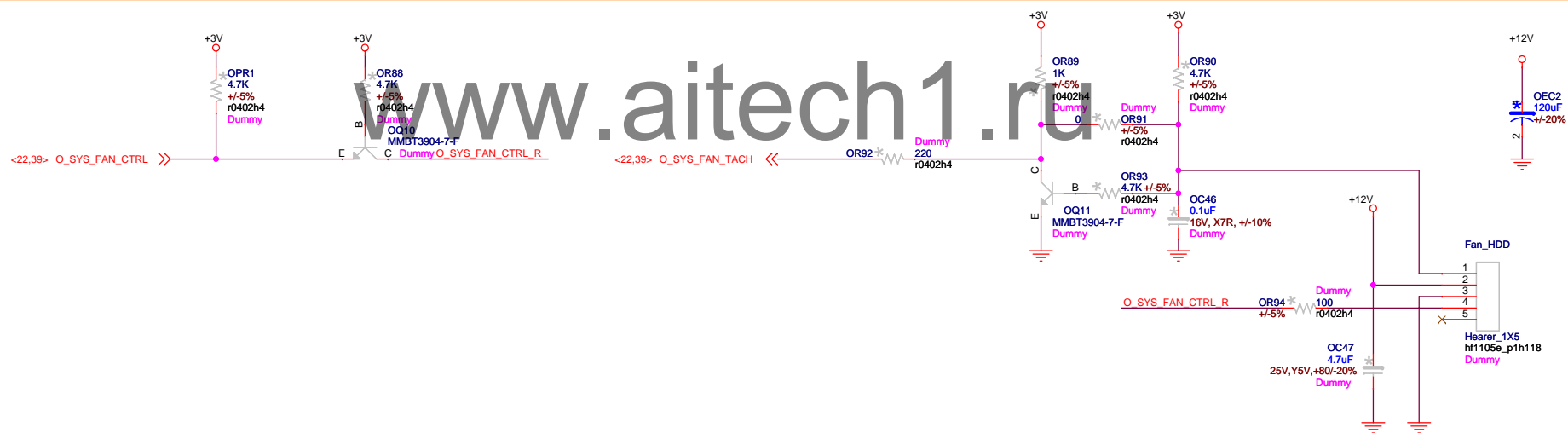
CONN-D-SUB



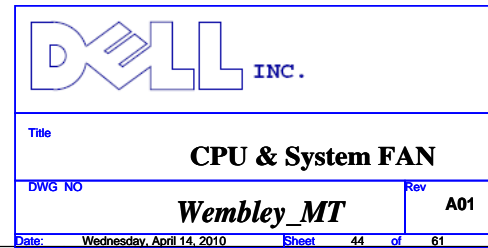
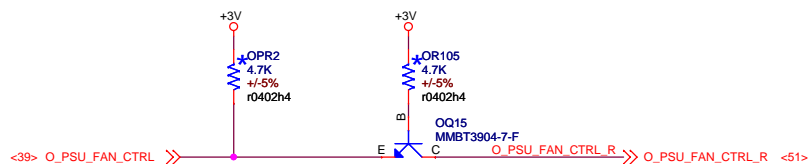
CPU Fan

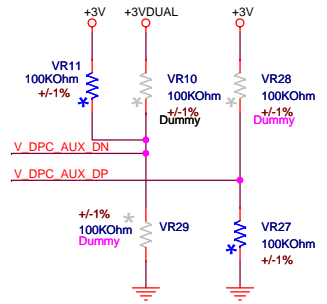
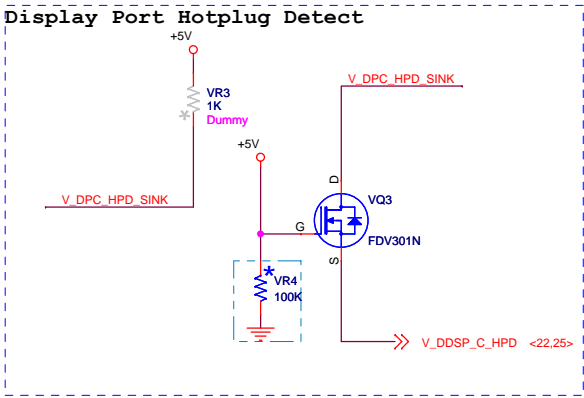
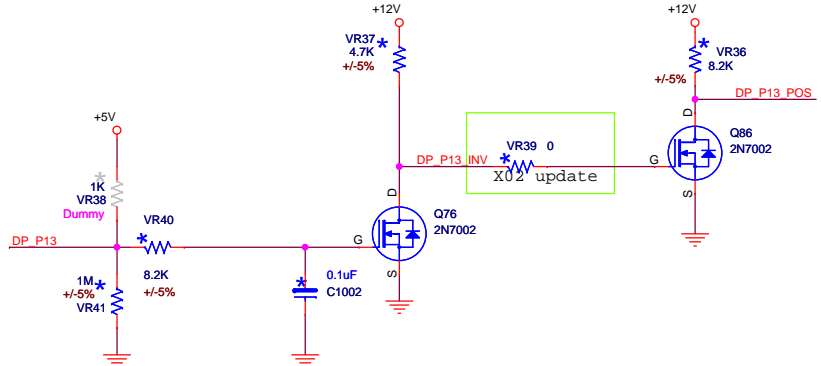
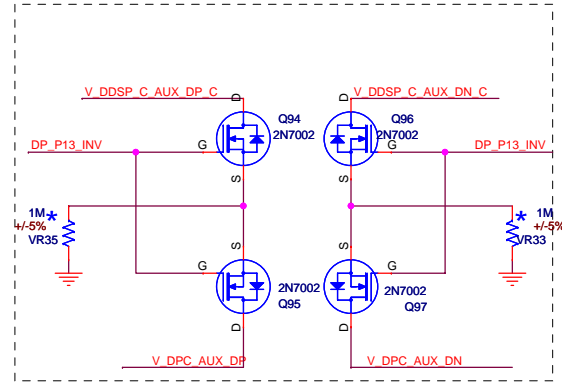
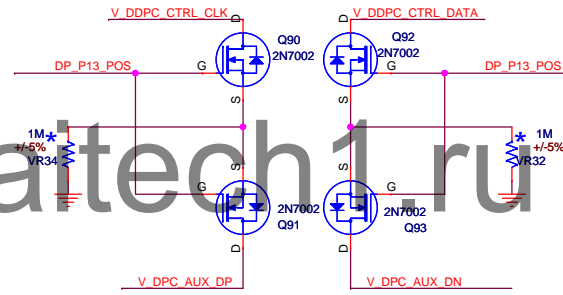
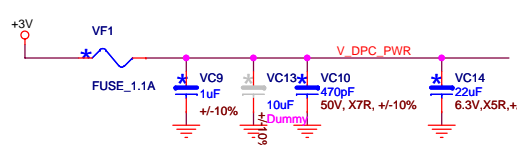
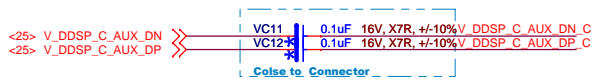
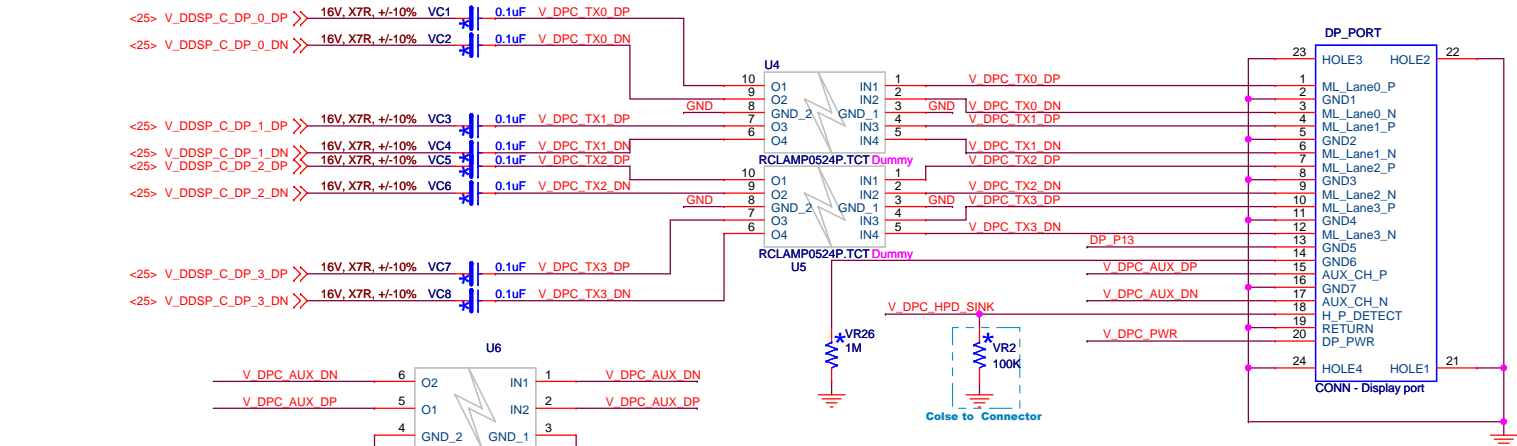



SYS Fan



PSU Fan







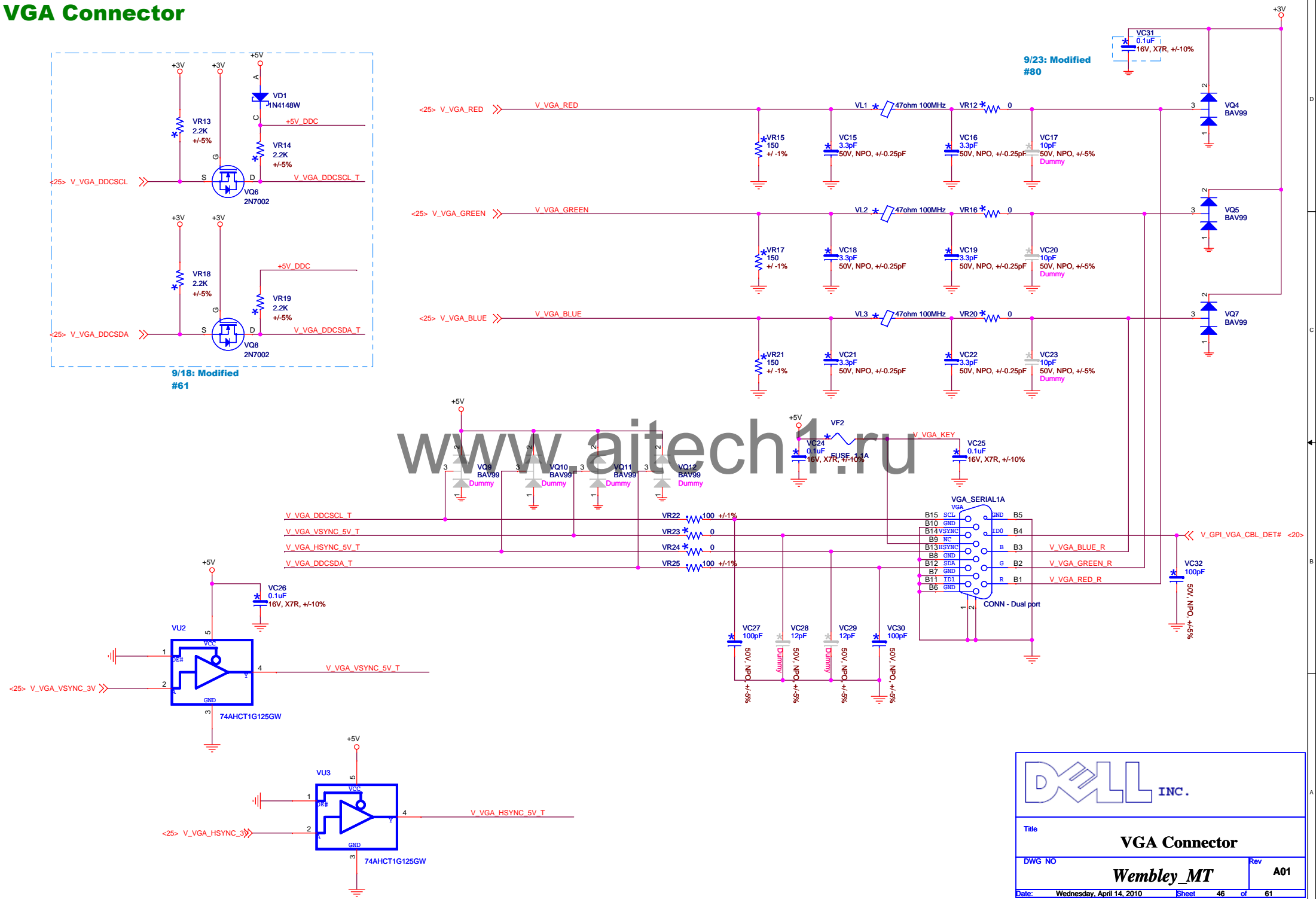
DISPLAY PORT

Wembley_MT

A01

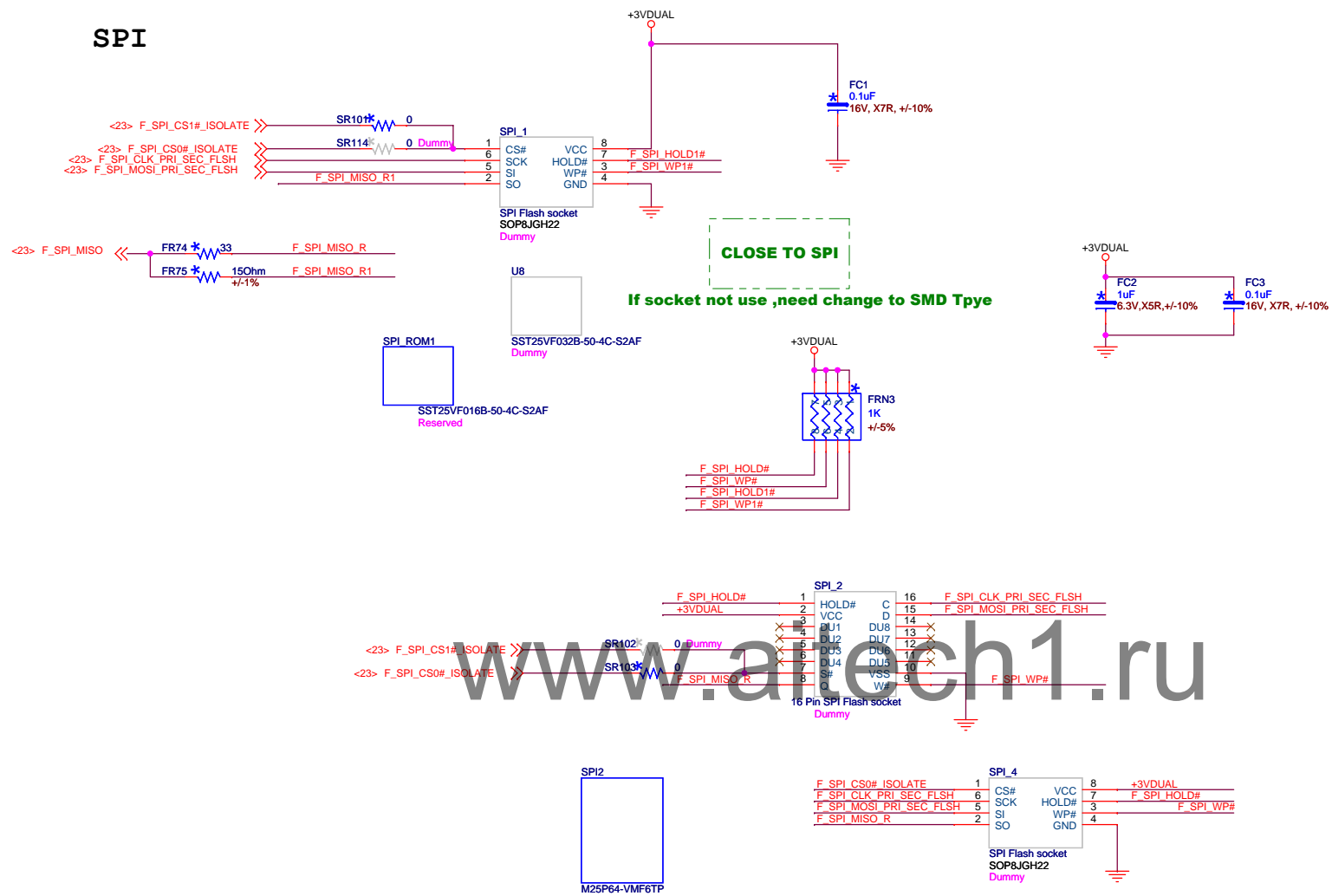
Date: Wednesday, April 14, 2010 Sheet 45 of 61

VGA Connector



Title		VGA Connector	
DWG NO		Wembley_MT	
Date: Wednesday, April 14, 2010		Sheet	46 of 61
		Rev	A01

SPI

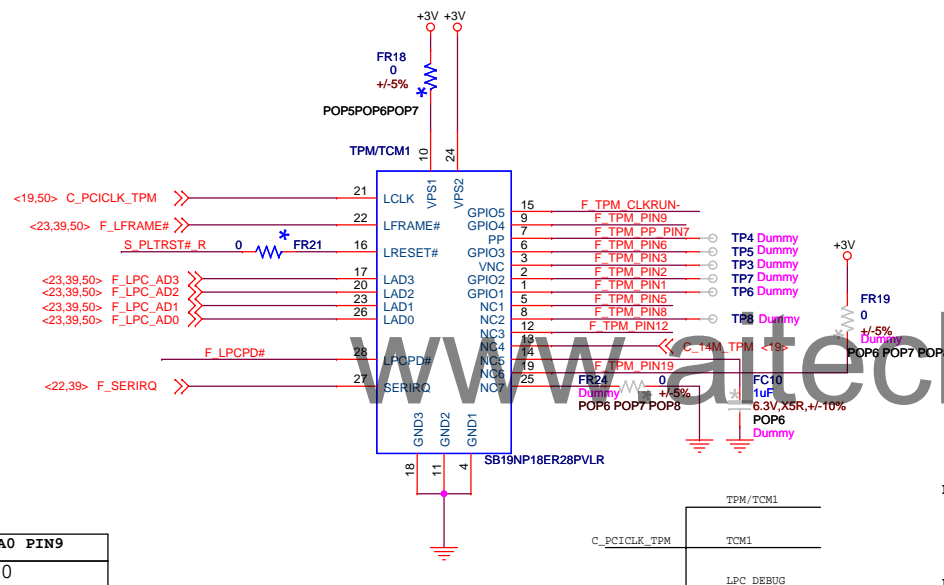
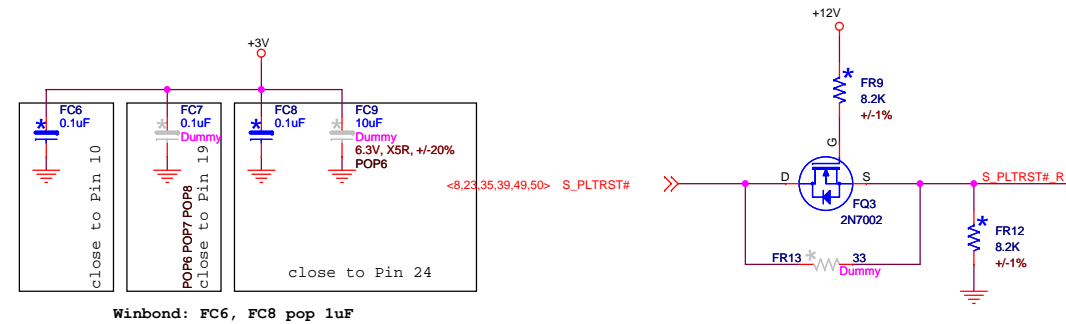


TPM, TCM

(Default) ST Micro	POP5	FR18,FR32,FR37
ZTE	POP6	FR18,FR24,FR32,FR35,FR36,FR37,FC7,FC9,FC10,FC11,FC12,FR19
Jetway	POP7	FR18,FR24,FR29,FR32,FR37,FC7,FR19
Winbond	POP8	FR24,FR26,FR27,FR37,FC7,FC15,FR19

14Mhz Clock Option Table (from CK.GEN or PCH)

(Default) ST Micro	From CK.GEN.	No Stuff CR98,CR194	From PCH	No Stuff CR198
ZTE	From CK.GEN.	No Stuff CR98,CR194	From PCH	No Stuff CR198
Jetway	From CK.GEN.	Stuff CR98,CR194	From PCH	Stuff CR198
Winbond	From CK.GEN.	No Stuff CR98,CR194	From PCH	No Stuff CR198

Z

Base Address	BA1 PIN3	BA0 PIN9
EE / EF	0	0
7E / 7F	0	1
2E / 2F	1	0
4E / 4F	1	1

Default set EE/EF as Amy recommended,
Pin 3 and Pin 9 have internal PU in Z.

J

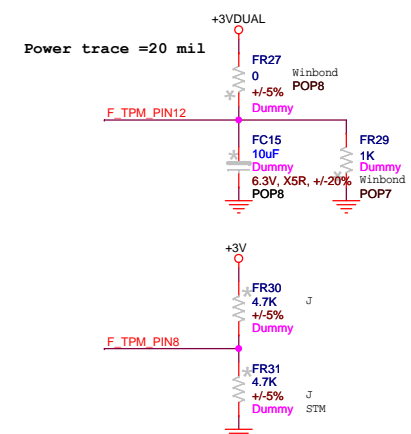
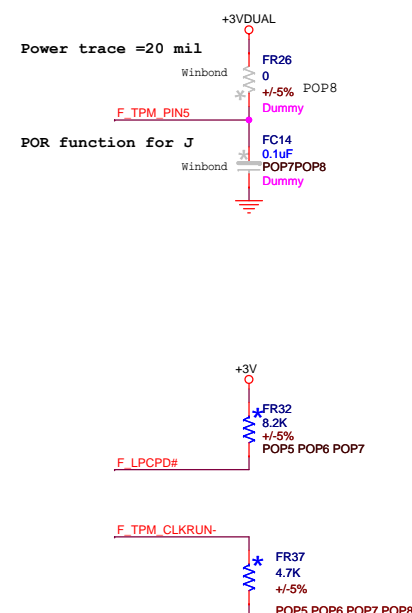
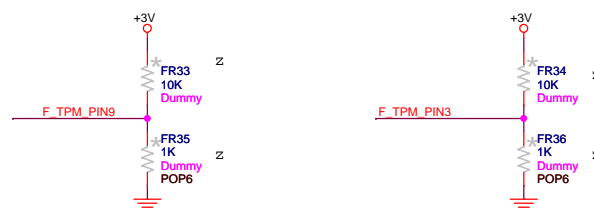
STATUS	TESTEN PIN8	RUNMODES PIN5
NORMAL MODE	0	X
JTAG MODE	1	0
NORMAL MODE	1	1

J has internal PD with PIN8,
internal PU with PIN9

J

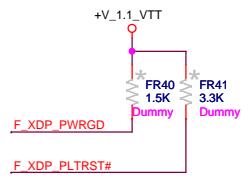
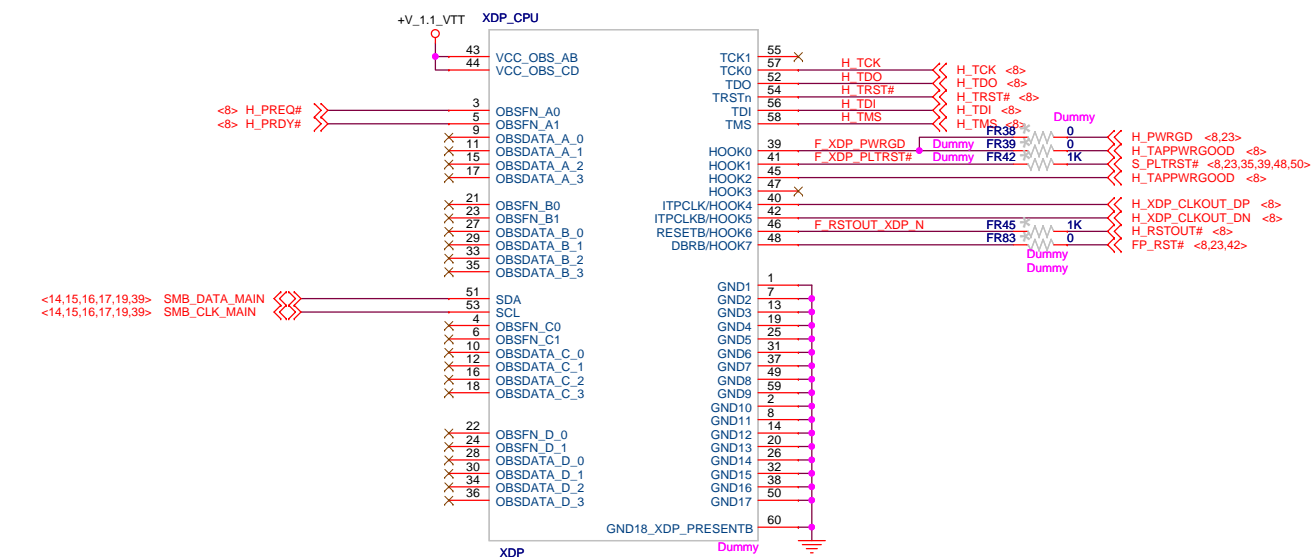
	1(default)	0
BSEL PIN12	FLASH	SRAM

J has internal PU with PIN12

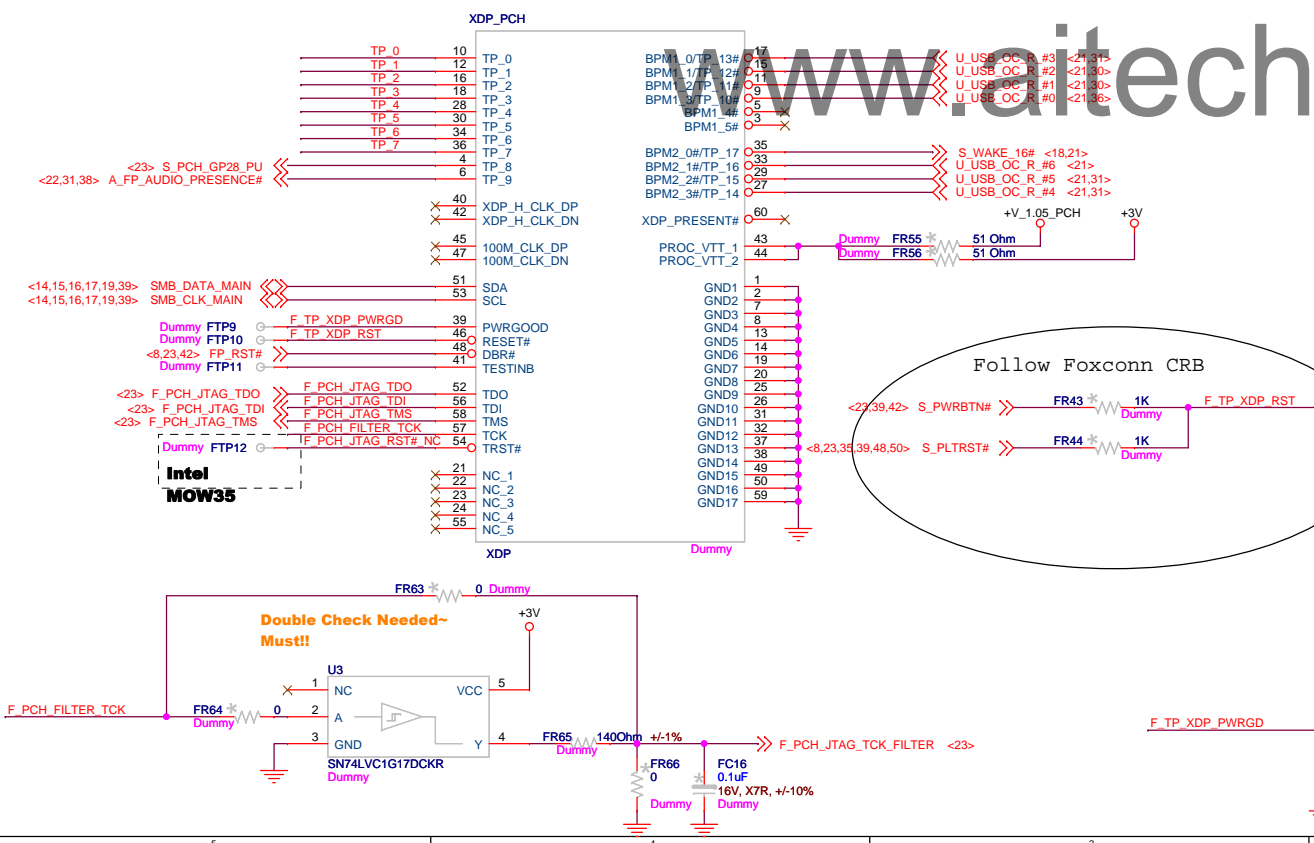


Title			
TPM & TCM			
DWG NO	Wembley_MT		Rev A01
Date: Wednesday, April 14, 2010	Sheet	48 of	61

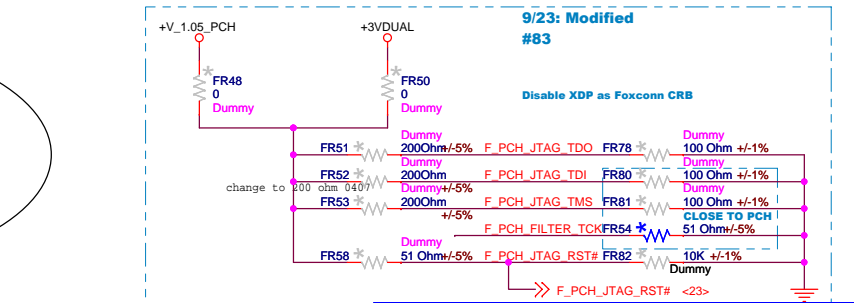
XDP Connector - CPU




XDP Connector - PCH



WW35 2008 recommend		PCH JTAG Enable		PCH JTAG Disable	
		ES1	ES2	ES1	ES2
F_PCH_JTAG_TDO	R51	No Stff	200 Ohms ¹	No Stuff	No Stuff
	R78	No Stff	100 Ohms ¹	No Stuff	No Stuff
F_PCH_JTAG_TMS	FR53	200 Ohms	200 Ohms	No Stuff	No Stuff
	FR81	100 Ohms	100 Ohms	No Stuff	No Stuff
F_PCH_JTAG_TDI	FR52	200 Ohms	200 Ohms	20K Ohms	No Stuff
	FR80	100 Ohms	100 Ohms	10K Ohms	No Stuff
F_PCH_FILTER_TCK	FR54	51 Ohms	51 Ohms	51 Ohms	51 Ohms
	FR58	20K Ohms	20K Ohms	No Stuff	No Stuff
F_PCH_JTAG_RST#	FR82	10K Ohms	10K Ohms	No Stuff	No Stuff



INC.

Title

XDP

DWG NO

Wembley_MT

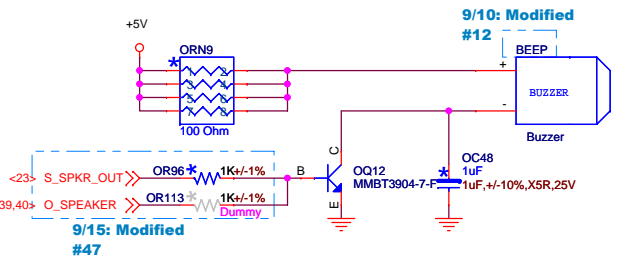
Date: Wednesday, April 14, 2010

Sheet 49 of 61

Rev

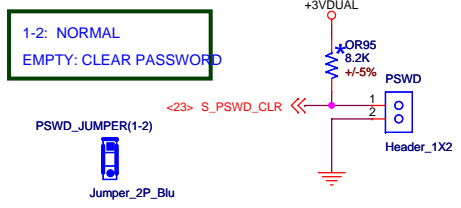
A01

BEEP



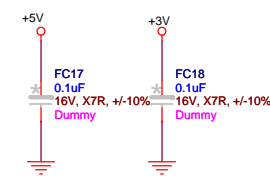
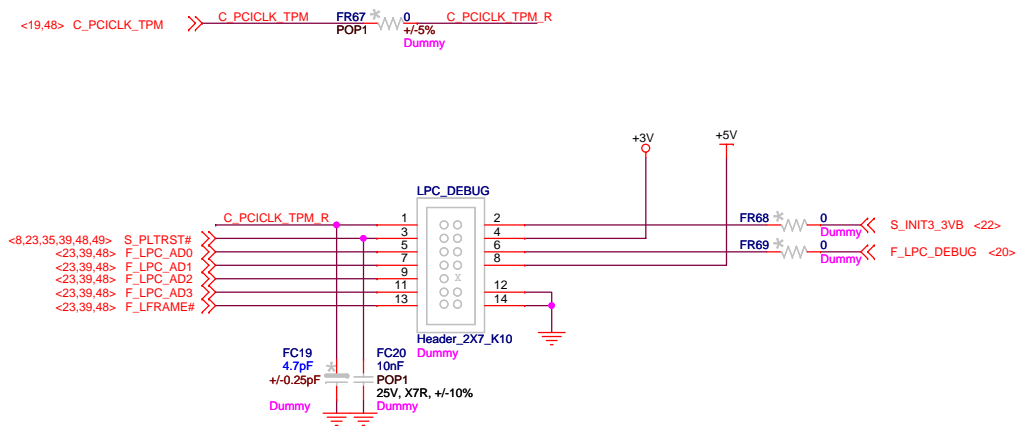
MISC Connector


Clear Password



LPC DEBUG

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**INC.**

BUZZER / CLR PSWD /LPC DEBUG

DWG NO

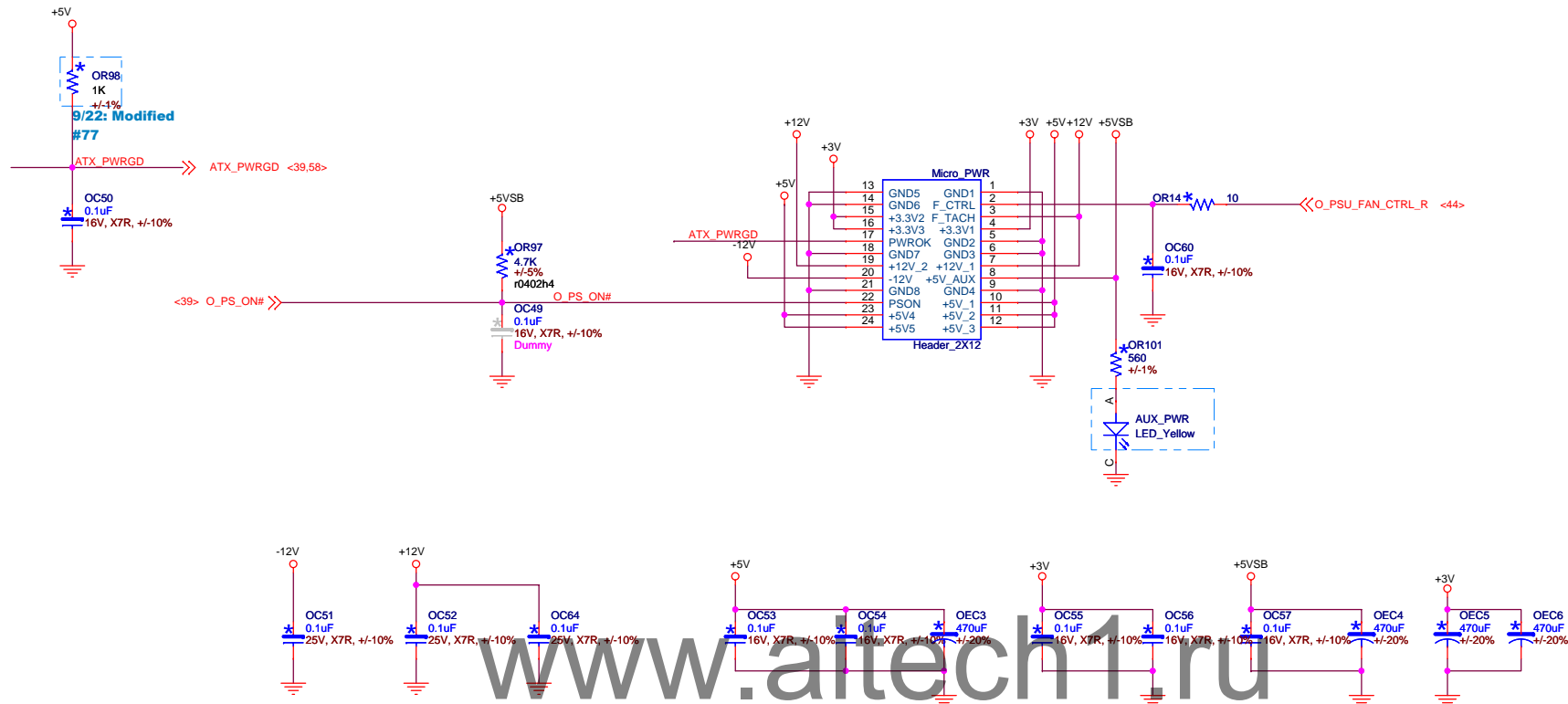
Wembley_MT

Date: Wednesday, April 14, 2010

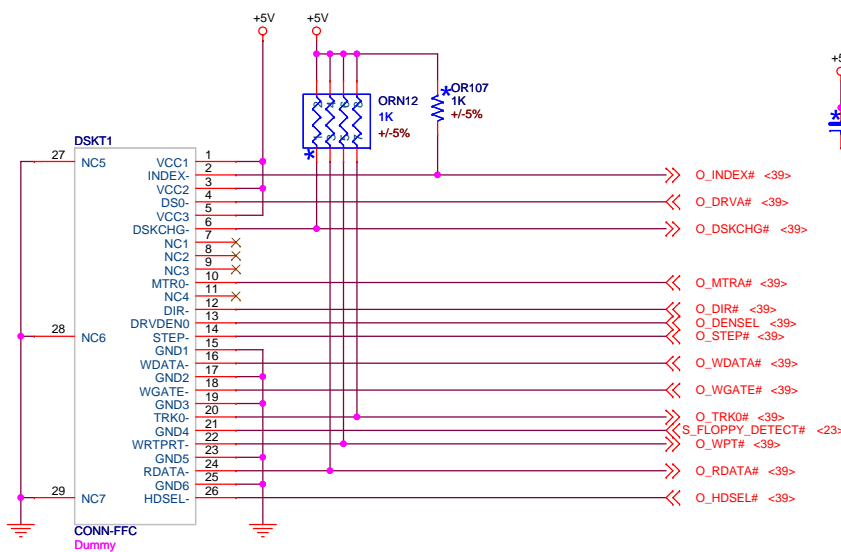
Sheet 50 of 61

Rev A01

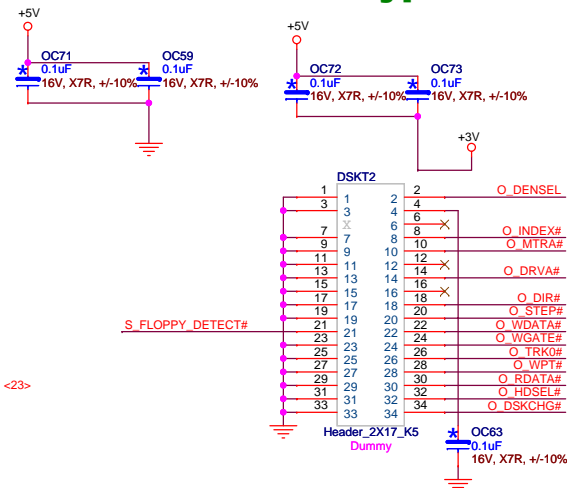
ATX POWER CONNECTOR



Slim Type @ SFF



Standard Type @ DT



Title		
ATX POWER CONN /FDD		
DWG NO	Rev	
	A01	
Date:	Wednesday, April 14, 2010	Sheet 51 of 61

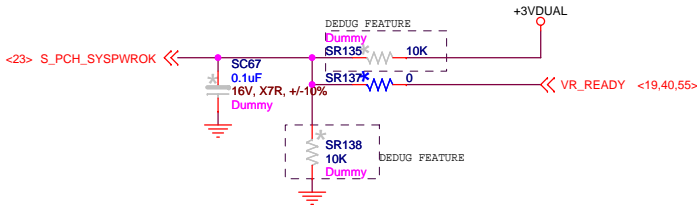
BACKFEED CUT

9/24: Modified #93
Remove LATCHED BACKFEED CUT Circuit

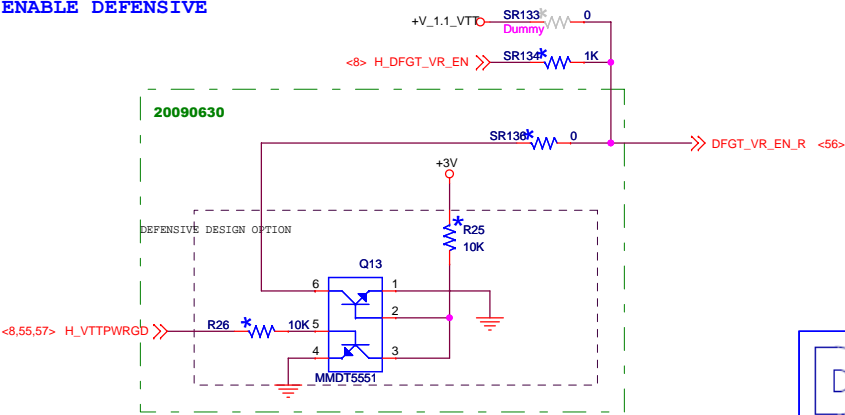
9/12: Modified #42
Remove PCIE RESET Control
Circuit

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VR_READY DEFENSIVE (PCH POWEROK)

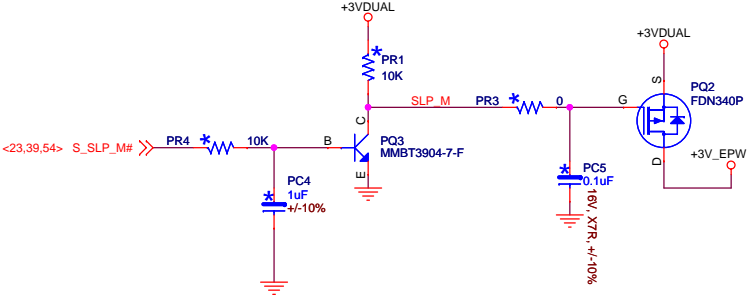


GFX VR ENABLE DEFENSIVE

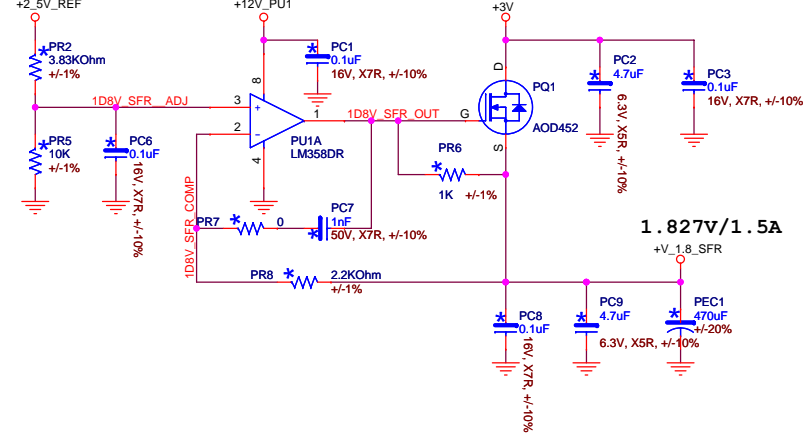


Title	
POWER SEQUENCE	
DWG NO	Rev
Wembley_MT	A01
Date: Wednesday, April 14, 2010	Sheet 52 of 61

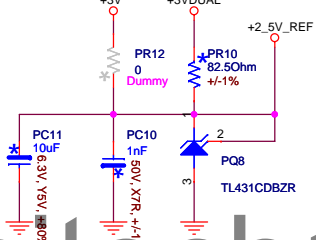
+3V_EPW(FOR PCH ME)



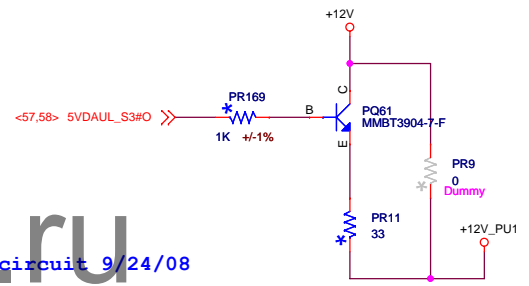
+V_1.8_SFR



+2.5V Ref for OP(PU1)



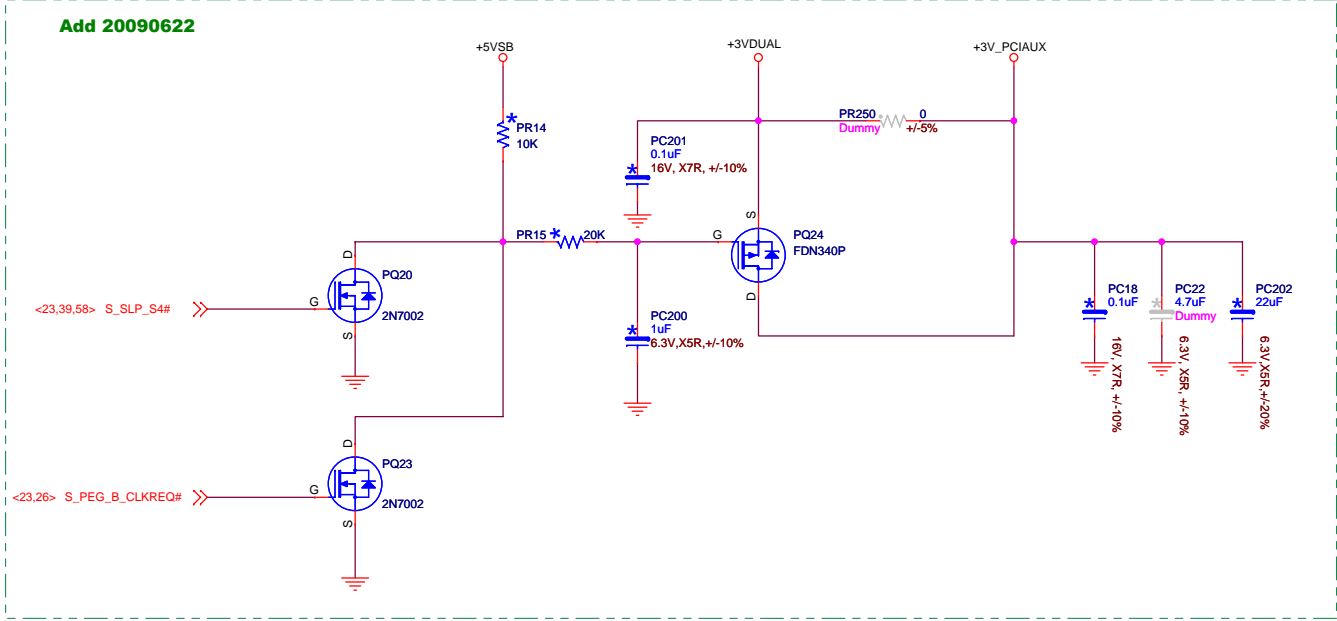
Control OP(PU1) turn on/off sequence



www.aitech1.ru Add circuit 9/24/08

+3V_PCIAUX(FOR PCI/PCIE SLOT)

Add 20090622



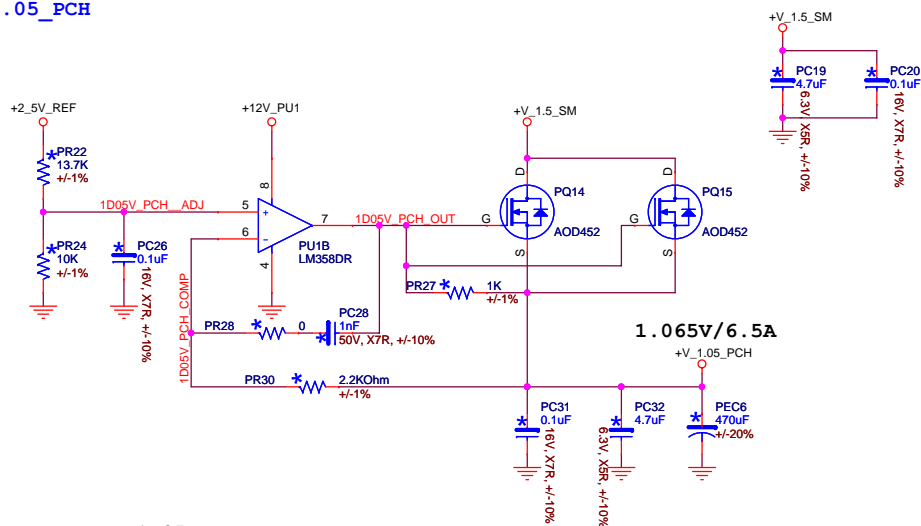
DELL INC.

Title: **POWER-1:LINEAR POWER-1**

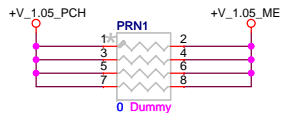
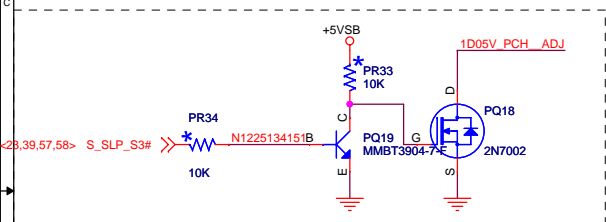
DWG NO: **Wembley_MT** Rev: **A01**

Date: Wednesday, April 14, 2010 Sheet 53 of 61

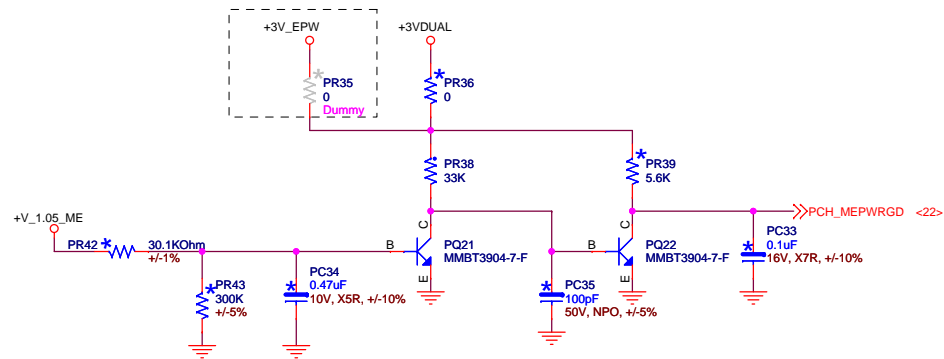
+V_1.05_PCH



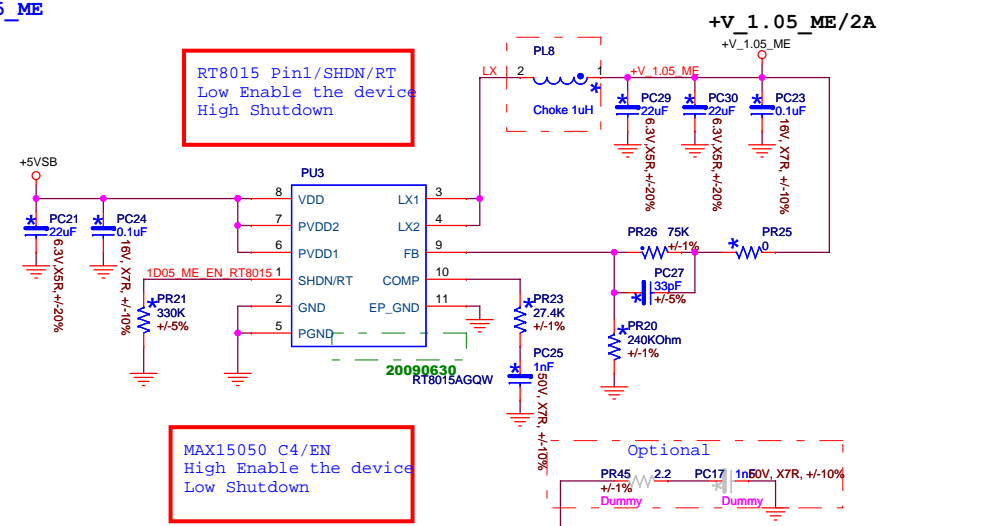
+V_1.05_PCH
ENABLE CIRCUIT



+3V_EPW RACE CONDITION DEFENSIVE



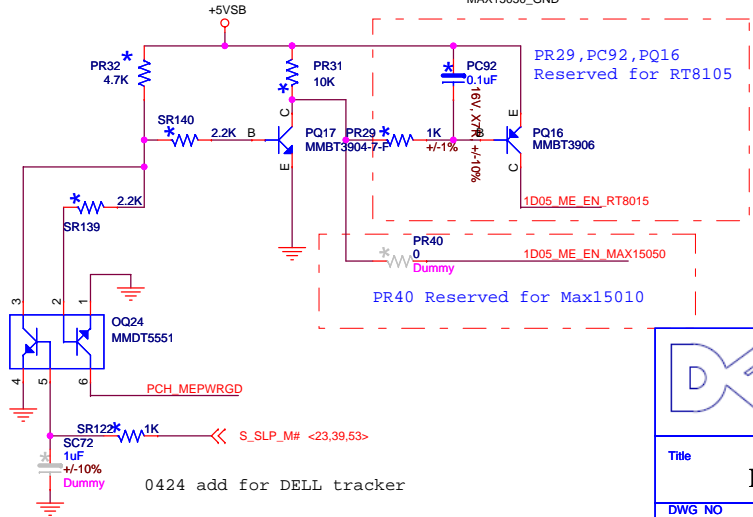
+V_1.05_ME



RT8015 Pin1/SHDN/RT
Low Enable the device
High Shutdown

MAX15050 C4/EN
High Enable the device
Low Shutdown

+V_1.05_ME
ENABLE CIRCUIT



DELL INC.

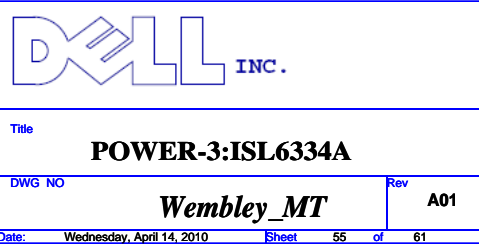
Title: **POWER-2:LINEAR POWER-2**

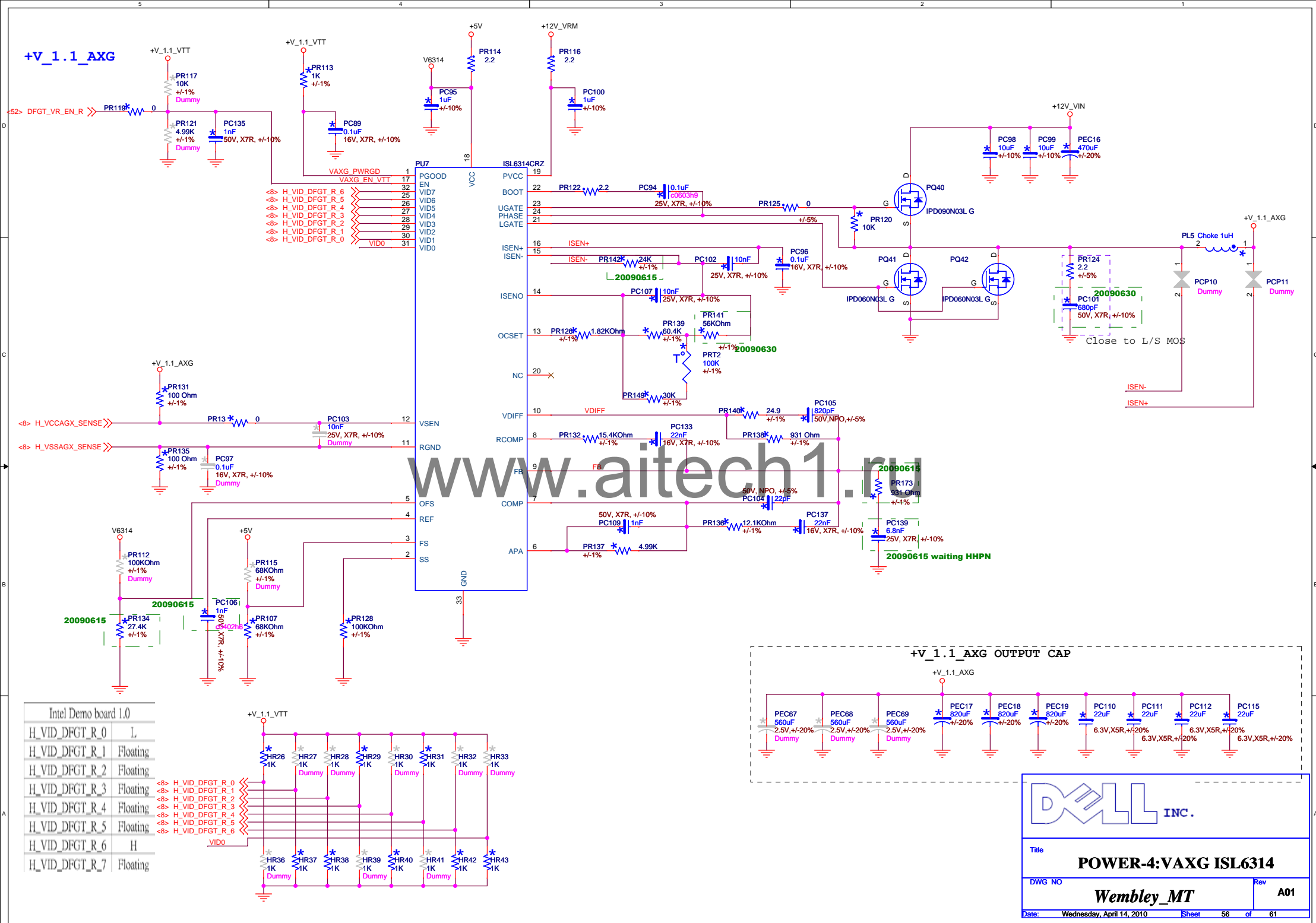
DWG NO: **Wembley_MT**

Date: **Wednesday, April 14, 2010**

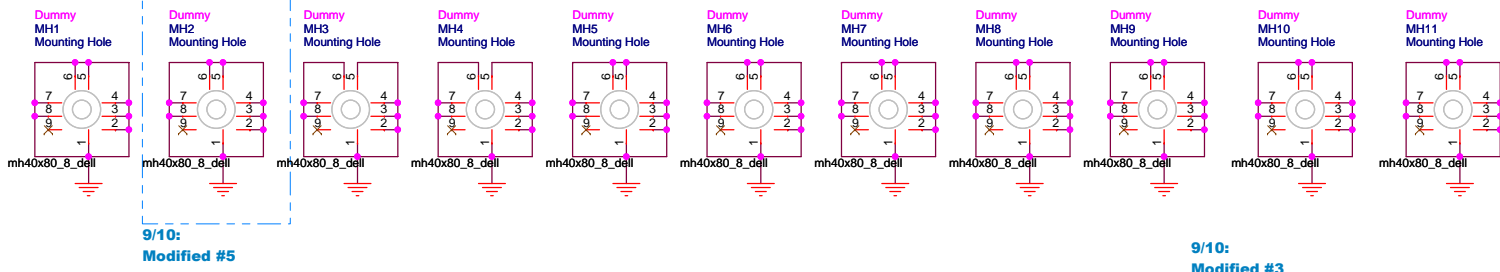
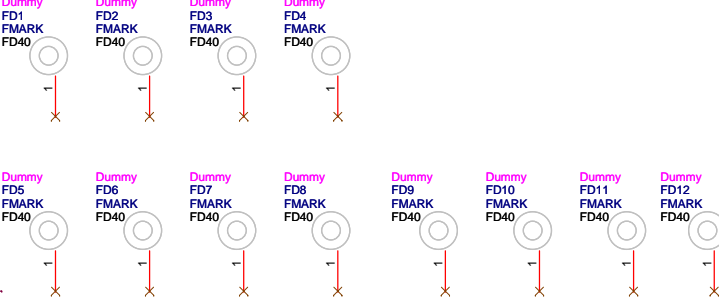
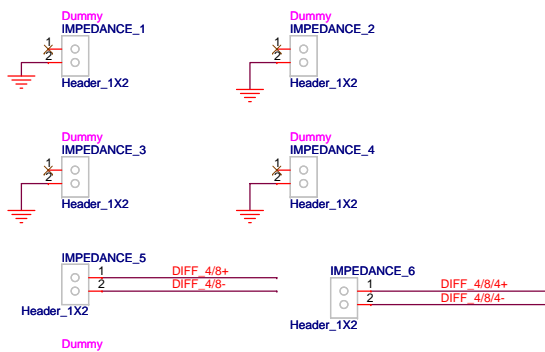
Sheet: **54** of **61**

Rev: **A01**

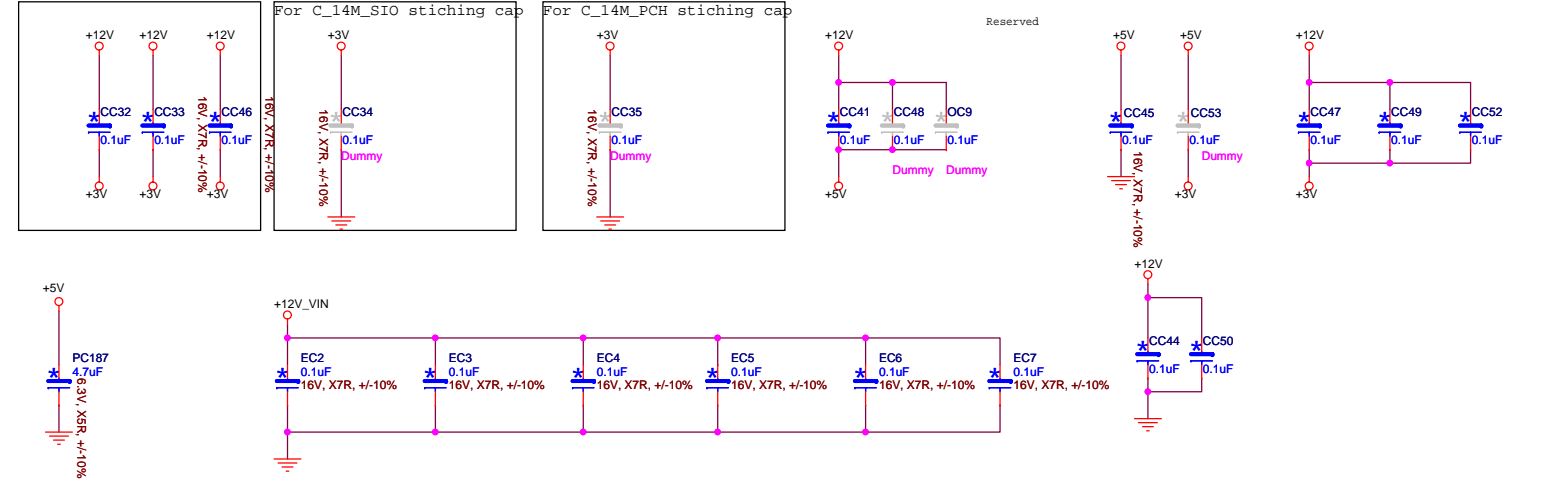
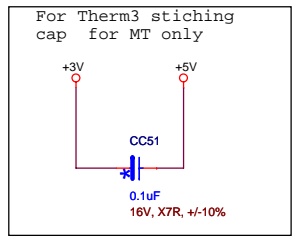
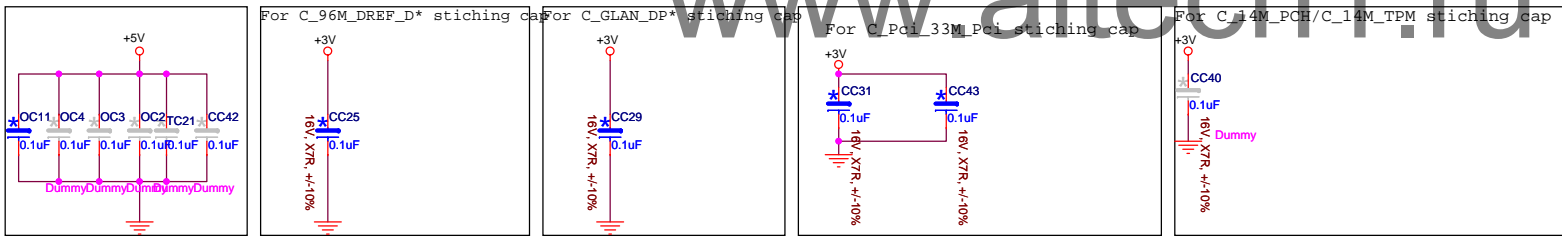




Intel Demo board 1.0	
H_VID_DFGT_R_0	L
H_VID_DFGT_R_1	Floating
H_VID_DFGT_R_2	Floating
H_VID_DFGT_R_3	Floating
H_VID_DFGT_R_4	Floating
H_VID_DFGT_R_5	Floating
H_VID_DFGT_R_6	H
H_VID_DFGT_R_7	Floating



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Title		EMI	
DWG NO	Wembley_MT		Rev
		A01	
Date:	Wednesday, April 14, 2010	Sheet	59 of 61

X00 → X01 Change list

1.Dummy VQ10,VQ11,CR98,CR99,CR194,CR196
2.Stuff CR191,CR193
3.Update Page 60 GPIO form
4.Add SPI_ROM1 (SST25VF016B-50-4C-S2AF)
5.Stuff C541. CR12 change to 22ohm.
6.Update PCH P/N for B0 stepping. Chipset,BD82IBX,B0,QLLS,FCBGA,951P,G
7.Stuff SR41
8.Un-stuff FR48 , stuff FR50
9.FR51,FR52,FR53 change to 200ohm
10.SR126 change to 0ohm SMD 0402
11.CR96 change to 18 ohm SMD 0402.
12.ChassID [2:0] SFF=101 / DT=100 / MT = 000
13.SPI_ROM1 (2M) and SPI2 (8M) BOM stuff
14.Modify RSMRST# circuit.
15.Add OQ26(3904) ,SR105,SR188,SR187
16.Change ME_PWRGD and SLM_M# circuit. 1.PR32 change from 10K to 4.7K 2.Delete PR37 3.Add SR140 2.2K 0402 4.SR139 change to 2.2K
17.Delete LD1 (BAT54A) , Add LU1 (AND gate) , L1C33
18.Stuff CR114
19.SR73 change to 1.1K 0603 , SR76 change to 3.01K 0402
20."Delete net K_PCIRST# at PCH section. (Keep net SIO to PCI Slot)
"
21.Delete SIO5544 SPI interface (SIO update datasheet)
22.28.Change CPU to VREF connection to remove long stub to D3R30/29 and D3R9,D3R11.
23.No Stuff SR98
24."PQ26,PQ29,PQ32,PQ35,PQ43,PQ44 change to NTMFS4943NT1G
"
25."PQ27,PQ28,PQ30,PQ31,PQ33,PQ34,PQ36,PQ37,PQ45,PQ46 change to NTMFS4939NT1G
"
26."PU1 change to LM358DR
"
27.Stuff CC25,CC29,OC11,CC31,CC43,CC41,CC45,CC47,CC49,CC52,CC50,CC44,CC32,CC33,CC46,EC7,EC6,EC5,EC4,EC3,EC2. for EMC.
28.No Stuff CC35,CC34,OC4,OC3,OC2,TC21,CC42OC9,CC48,CC53 for EMC.
29.DIMM Vref follow MOW (stuff D3R9,D3R31,HR83,HR84)
30.VGA buffer VU2,VU3 change to 74LVC1G125 . VR23,VR24 change to22.6 ohm
31.No stuff SL1,SL2,SL4,SL6,SR123,SR125,SR127,SR130,SC35,SC36,SC42,SC48,SC53,SC54 for remove LC Filter on VccAC1k, Vccap11EXP, VccFDIPLL, and VccSATAPLL.
32.OU2 RS232 Driver IC Change to TI SN200602074PWR
33."1CR106 change to 18 ohm SMD 0402.
2.FC19 change to 5pF"
34.RTC caps SC8,SC9 change to 10pF
35.3. Change AR1/2 from 57.6 to 90-Ohm. (Improve HP-OUT 32-Ohm's Cross-Talk and THD+N).
36.No Stuff Floppy connector
37.Need to move O_IO_PME# from GPIO13 to RI# input on PCH
38.Move X1_WAKE from GPIO5 to GPIO13 input on PCH to have wake capability
39.Move X4_WAKE from GPIO34 to GPIO11 (SMBALERT) input on PCH to have wake capability
40.add 1000pF cap to PQ54 gate to GND for ESD issue.
41.Add OC12 (Dummy) for EMI , place near SIO pin123
42.PCH 120Mhz Clock No use (tie to GND) for MOW23 Add HR1,HR2 0 ohm 0402 , Dummy CR172,CR173
43.Add VR10 pull high 3VDUAL for MOW 16 update (BOM stuff VR11 for PU 3V)
44.JTAG Follow CRB . FR58 change to 51 ohm (Dummy) , FR82 change to 10K ohm (Dummy)
45.Issue with MEPWR and GPIO60, Please use PCH GPIO74 and rename to MFG_MODE_OVERRIDE#
46.Change value of L1C32 to 0.1uF. For EMI
47.Add 0.1uF OC74,OC75 (Dummy) Caps on Pins-4 and 5 of FAN_CPU connector. For EMI
48.AU3 change P/N to ALC269-VB
49.No stuff AD5,AD6,AR61,AR62,AU2 for ALC269-VB
50.Stuff AC67 , FB4 (0 ohm) for ALC269-VB
51.Dummy R55 , Stuff R54 for ALC269-VB
52.Add +3V PCIVAUX for EPU 1W control (Slot AUX power)
53.Add AR74,AR75 SMT 0603 for DELL tracker
54.Add L1R49 , L1C34 for 3VDUAL Drop issue
55.Del ACP1,ACP2,ACP3 for Audio Layout
56.Move AR44 to AR69 for Relatek Class-D power down.
57.Update DC/DC for +3V PCIVAUX (use GPIO 56)
58.Audio Caps AC25,26,27,28 and AC38,39,40,41 expected to decouple to DGND (not AGND)
59.Change Screw Hole foot print mh40x80 8 dell
60.Connect MFG_MODE_OVERRIDE back to GPIO74, and connect SPK_MUTE# back to GPIO73.
Please use a MMBT3904 to create an inverter to use in place of the diode going between MFG_MODE_OVERRIDE and MFG_MODE.
Add OQ27,SR34
61.Add UC20,UC21 0.1uF 0402 for EMI
62.AR66 , AR67 stuff 1210 0ohm for DFM issue
63.SFB1 change to 0 ohm for Intel MOW
64.Stuff USB common choke , no stuff 0 ohm (Stuff UL1,UL2,UL3,UL4,UL7,UL8,UL9,UL10UL11,UL12,UL13,UL14)
(No stuff UR1,UR2,UR5,UR6,UR7,UR8,UR10,UR12,UR33,UR34,UR35,UR36,UR21,UR22,UR23,UR24,UR37,UR38,UR41,UR42)
65.Add CC51 for Therm3 EMI cross moat. (For MT only , SFF no cross moat)
66.MT PC193 rename AC21 PC194 rename AC22
67. No stuff CR198 for TPM 14Mhz as default . 68. Change SR134 to 1K ohm. PR119 change to 0 ohm for Power.

X01 → ENG3 Change list


1. change OEC6 P/N: 621207Y00-021-G for DFM issue
2. no stuff Braidwood (ONFI1), intel no suport
3. change PCH HS:Foxconn Heatsink
4. change FC19 to 4.7p for EIV CLK issue
5. C541 change 10pF CR12 change 22ohm meet PCH chip Cin
for EIV measure
6. TPM change P/N ST,ST19NP18ER28PVMS
7. power connect need change(micro_pwr)HM4212E-D

ENG3 → X02 Change list

1. change Audio version ALC269Q-VB3-GR
2. (remove jtag) FR52,FR53,FR80,FR81 for EUP1W
3. (AUXLED)OR101 change 560 ohm
4. SFF USB port 10 port11 nostuff ,so nostuff UL13, UL14,UC18,UEC7, UF7,UR39,UR40,UC19 , stuff SR7
5. AR1 AR2 change to 22 ohm, for for HP FSOV w/ 300ohm load (> 1Vrms).
6. AC21 AC22 change to 22uF/1206/6.3V for THD+N at low freq
7. No Stuff D3C49, D3U4, D3R32, D3R28,D3R26,D3R25,D3C50, D3U1, D3C47, D3R27, D3R29, D3C48, D3R12, D3R15, D3U2, D3R13, D3R16, D3C38, D3C36, D3R10, D3R14, D3C37, ONFI1, SR172, SR173, THRM1, THRM2, OR108, PWR_SWH, OR114, RST_SWH, Fan HDD, OR94, OR98, OR90, OC46, OR93, OQ11, OR92, OPR1, OR88, OQ10,XDP_CPU, FR38, FR40, FR42, FR45, FR83, XDP_PCH, FR55, FR63, FR60, FR50, FR52, FR53, FR80, FR81 for Drew mail
8. S_WAKE# connect to GPIO 14(Original is PCH Pin AR23 Wake#)


A00 Change list

1. Change VR23/VR24 from 22.6 ohm to 0 ohm (0603).
2. No Stuff VC28/VC29 .
3. Change VU2/VU3 to ON M74VHC1GT125DF2G

	
Title Change_list	
DWG NO Wembley_MT	Rev A01
Date: Wednesday, April 14, 2010 Sheet 60 of 61	

Name	Type	Tolerance	Power Well	Default	Blink Capability	Description	Schematic Usage
GPIO75	I/O	3.3 V	Suspend	Native	No	SML1DATA	S_SMLINK1_DATA
GPIO74	I/O	3.3 V	Suspend	Native	No	SML1ALERT#	MFG_MODE_OVERRIDE#
GPIO73	I/O	3.3 V	Suspend	Native	No	Multiplexed with PCIECLKREQ0#	SPK_MUTE#
GPIO72	I/O	3.3 V	Suspend	Native (Mobile)	No	Mobile: Multiplexed with BATLOW#. Desktop: Unmultiplexed (Note 4)	S_GPI_SKU3
GPIO67	I/O	3.3 V	Core	Native	No	Multiplexed with CLKOUTFLEX3	S_TP_CLKOUTFLEX3
GPIO66	I/O	3.3 V	Core	Native	No	Multiplexed with CLKOUTFLEX2	
GPIO65	I/O	3.3 V	Core	Native	No	Multiplexed with CLKOUTFLEX1	S_TP_CLKOUTFLEX1
GPIO64	I/O	3.3 V	Core	Native	No	Multiplexed with CLKOUTFLEX0	S_TP_CLKOUTFLEX0
GPIO63	I/O	3.3 V	Suspend	Native	No	Multiplexed with SLP_S5#	S_TP_SLP_S5#
GPIO62	I/O	3.3 V	Suspend	Native	No	Multiplexed with SUSCLK	S_TP_SUSCLK
GPIO61	I/O	3.3 V	Suspend	Native	No	Multiplexed with SUS_STAT#	S_LPCPD#
GPIO60	I/O	3.3 V	Suspend	Native	No	Multiplexed with SML0ALERT#	S_SMLALERT
GPIO59	I/O	3.3 V	Suspend	Native	No	Multiplexed with OC[0]# (Note 12)	U_USB_OC_R_#0
GPIO58	I/O	3.3 V	Suspend	Native	No	Multiplexed with SML1CLK	S_SMLINK1_CLK
GPIO57	I/O	3.3 V	Suspend	GPI	No	Unmultiplexed	S_TPM_PHY_PRESENT
GPIO56	I/O	3.3 V	Suspend	Native	No	Multiplexed with PEG_B_CLKREQ#	S_PEG_B_CLKREQ#
GPIO55	I/O	3.3 V	Core	Native	No	Multiplexed with GNT3#	K_PCI_GNT3#
GPIO54	I/O	5.0 V	Core	Native	No	Multiplexed with REQ3# (Note 12)	K_PCI_REQ3#
GPIO53	I/O	3.3 V	Core	Native	No	Multiplexed with GNT2#	K_PCI_GNT2#
GPIO52	I/O	5.0 V	Core	Native	No	Multiplexed with REQ2# (Note 12)	K_PCI_REQ2#
GPIO51	I/O	3.3 V	Core	Native	No	Multiplexed with GNT1#	K_PCI_GNT1#
GPIO50	I/O	5.0 V	Core	Native	No	Multiplexed with REQ1# (Note 12)	K_PCI_REQ1#
GPIO49	I/O	3.3V	Core	GPI	No	Multiplexed with SATA5GP	S_PCH_CONFIG_JUMPER
GPIO48	I/O	3.3 V	Core	GPI	No	Multiplexed with SDATAOUT1	S_MT_USB_HDR_CBL_DET#
GPIO47	I/O	3.3V	Suspend	Native	No	Multiplexed with PEG_A_CLKREQ#	S_PEG_A_CLKREQ#
GPIO46	I/O	3.3V	Suspend	Native	No	Multiplexed with PCIECLKREQ7#	S_PCIECLKREQ#7
GPIO45	I/O	3.3V	Suspend	Native	No	Multiplexed with PCIECLKREQ6#	S_PCIECLKREQ#6
GPIO44	I/O	3.3V	Suspend	Native	No	Multiplexed with PCIECLKREQ5#	S_PCIECLKREQ#5
GPIO43	I/O	3.3 V	Suspend	Native	No	Multiplexed with OC[4:1]# (Note 12)	U_USB_OC_R_#4
GPIO42	I/O	3.3 V	Suspend	Native	No		U_USB_OC_R_#3
GPIO41	I/O	3.3 V	Suspend	Native	No		U_USB_OC_R_#2
GPIO40	I/O	3.3 V	Suspend	Native	No	U_USB_OC_R_#1	U_USB_OC_R_#1
GPIO39	I/O	3.3 V	Core	GPI	No	Multiplexed with SDATAOUT0	A_FP_AUDIO_PRESENCE#
GPIO38	I/O	3.3 V	Core	GPI	No	Multiplexed with SLOAD	S_GPI_CHASSIS_ID2
GPIO37	I/O	3.3 V	Core	GPI	No	Multiplexed with SATA3GP	S_GPI_CHASSIS_ID1
GPIO36	I/O	3.3 V	Core	GPI	No	Multiplexed with SATA2GP	S_GPI_CHASSIS_ID0
GPIO35	I/O	3.3 V	Core	GPO	No	Multiplexed with SATACLKREQ#	S_GPI_SKU1
GPIO34	I/O	3.3 V	Core	GPI	No	Multiplexed with STP_PCIF	S_GPIO34
GPIO33	I/O	3.3 V	Core	GPO	No	Multiplexed with HDA_DOCK_EN# (Mobile Only) (Note 4)	S_MFG_MODE#
GPIO32	I/O	3.3 V	Core	GPO, Native (Mobile Only)	No	Unmultiplexed (Desktop Only) Mobile Only: Used as CLKRUN#, unavailable as GPIO (Note 4)	S_GPI_SKU0

Name	Type	Tolerance	Power Well	Default	Blink Capability	Description	Schematic Usage
GPIO31	I/O	3.3 V	Suspend	GPI	Yes	Multiplexed with ACPRESENT# (Note 7)	S_PSWD_CLR
GPIO30	I/O	3.3 V	Suspend	GPI	Yes	Multiplexed with SUS_PWR_DN_ACK Desktop: Cannot be used for native function. Used as GPIO30 only.	S_SUS_PWR_ACK
GPIO29	I/O	3.3 V	Suspend	GPI	No	Multiplexed with SLP_LAN# (Note 11)	L1_SLP_LAN#
GPIO28	I/O	3.3 V	Suspend	GPO	Yes	Unmultiplexed	S_PCH_GP28_PU
GPIO27	I/O	3.3 V	Suspend	GPO	Yes	Unmultiplexed	S_GP27_PD
GPIO26	I/O	3.3 V	Suspend	Native	Yes	Multiplexed with PCIECLKREQ4#	S_PCH_GP26_PD
GPIO25	I/O	3.3 V	Suspend	Native	Yes	Multiplexed with PCIECLKREQ3#	S_1_WATT_CTRL_1
GPIO24	I/O	3.3 V	Suspend	GPO	Yes	Unmultiplexed NOTE: GPIO24 configuration register bits are not cleared by CPH reset event.	S_FLOPPY_DETECT#
GPIO23	I/O	3.3 V	Core	Native	Yes	Multiplexed with LDRQ1#	L_DRQ1#
GPIO22	I/O	3.3 V	Core	GPI	Yes	Multiplexed with SCLOCK	S_GPI_BRD_REV1
GPIO21	I/O	3.3 V	Core	GPI	Yes	Multiplexed with SATA0GP	S_GPI_BRD_REV0
GPIO20	I/O	3.3 V	Core	Native	Yes	Multiplexed with PCIECLKREQ2#	S_FLEXBAY_HDR_CBL_DET#
GPIO19	I/O	3.3 V	Core	GPI	Yes	Multiplexed with SATA1GP	S_GPI_ESATA_DETECT#
GPIO18	I/O	3.3 V	Core	Native	Yes (Note 6)	Multiplexed with PCIECLKREQ1#	S_PCIECLKREQ#1
GPIO17	I/O	3.3 V	Core	GPI	Yes	Multiplexed with TACH0. Mobile: Used as GPIO17 only.	S_PCH_CPU_FAN_TACH
GPIO16	I/O	3.3 V	Core	GPI	Yes	Multiplexed with SATA4GP	H_SKTOCC_R_#
GPIO15	I/O	3.3 V	Suspend	GPO	Yes	Unmultiplexed	S_PCH_GP15
GPIO14	I/O	3.3 V	Suspend	Native	Yes	Multiplexed with OC7#	S_WAKE_16#
GPIO13	I/O	3.3 V	Suspend	GPI	Yes	Multiplexed with HDA_DOCK_RST# (Mobile Only) (Note 4)	X1_WAKE#
GPIO12	I/O	3.3 V	Suspend	GPI	Yes	Multiplexed with LAN_PHY_PWR_CTRL. GPIO Native functionality controlled via soft strap (Note 9)	L1_LAN_DISABLE#
GPIO11	I/O	3.3 V	Suspend	Native	Yes	Multiplexed with SMBALERT# (Note 12)	X4_WAKE#
GPIO10	I/O	3.3 V	Suspend	Native	Yes	Multiplexed with OC6# (Note 12)	U_USB_OC_R_#6
GPIO9	I/O	3.3 V	Suspend	Native	Yes	Multiplexed with OC5# (Note 12)	U_USB_OC_R_#5
GPIO8	I/O	3.3 V	Suspend	GPO	Yes	Unmultiplexed	S_IGC_EN#
GPIO7	I/O	3.3 V	Core	GPI	Yes	Multiplexed with TACH[3:2]. Mobile: Used as GPIO[7:6] only	S_GPI_SKU2
GPIO6	I/O	3.3 V	Core	GPI	Yes		S_GPI_PCH_HS_DET#
GPIO5	I/OD	5 V	Core	GPI	Yes	Multiplexed with PIRQ[H:E]# (Note 5).	S_USB_HDR_CBL_DET#
GPIO4	I/OD	5 V	Core	GPI	Yes	Multiplexed with PIRQ G	V_GPI_VGA_CBL_DET#
GPIO3	I/OD	5 V	Core	GPI	Yes	Multiplexed with PIRQ F	K_PCI_RISER_ID1
GPIO2	I/OD	5 V	Core	GPI	Yes	Multiplexed with PIRQ E	K_PCI_RISER_ID0
GPIO1	I/O	3.3 V	Core	GPI	Yes	Multiplexed with TACH1.	S_PCH_SYS_FAN_TACH1
GPIO0	I/O	3.3 V	Core	GPI	Yes	Multiplexed with BMBUSY#.	PECL_REQ#

		INC.	
Title			
GPIO PIN			
DWG NO		Rev	
Wembley_MT		A01	
Date: Wednesday, April 14, 2010		Sheet 61 of 61	